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ABSTRACT

All 16 Boolean logic functions in a single Ta/CoFeB/MgO device with perpendicular magnetic anisotropy were experimentally demonstrated based on the spin–orbit torque (SOT) effect. Furthermore, by combining with the voltage-controlled magnetic anisotropy (VCMA) effect, a novel SOT-MTJ (magnetic tunnel junction) prototype device with the assistance of the VCMA effect was further designed to perform magnetic field-independent logic operations. The numerical simulations were carried out, demonstrating the feasibility to realize all 16 Boolean logic functions in a single three-terminal device by applying the bias voltage and current injection as input variables. This approach provides a potential way toward the application of energy efficient spin-based logic, which is beyond the current von Neumann computing architecture.

The continued scaling of complementary metal-oxide-semiconductor (CMOS) technology according to Moore's law has brought to us upgraded electronic devices with a smaller volume, higher speed, and lower price for decades. However, the challenge to such rapid development still exists.[1,2] One critical limitation is the explosive growth of static power dissipation arising from the leakage current as the CMOS feature size scales down to a few nanometers.[3] On the other hand, the operating speed of electronic devices is seriously limited by the ineluctable data exchange between separate processor and memory units, encountering the so-called von Neumann bottleneck that further brings massive dynamic power dissipation.[4] To overcome the above-mentioned obstacles rooted in the existing Si-based electronic devices, new problem-solving strategies beyond CMOS or even beyond von Neumann are urgently needed and have aroused extensive research interests.[5,6]

One promising strategy is to introduce the emerging nonvolatile memories such as magnetoresistive memory,[7–12] resistive memory,[13–16] and phase-change memory[17] into logic circuits. Fortunately, due to their nonvolatile feature, these memories can eradicate the static power dissipation. More importantly, the exploration of their logic functions will lead to the unity of logic and memory units, hence thoroughly breaking the von Neumann bottleneck. In particular, the magnetic tunnel junction based on spin transfer torque (called the STT-MTJ) combines the advantages of nonvolatility, CMOS compatibility, and unlimited endurance,[18] showing great potential to construct a "stateful" logic circuit where intrinsic logic-in-memory cells both perform logic operations and store logic

values.[6] Recently, a reprogrammable logic gate consisting of three input STT-MTJs and one output STT-MTJ was designed to realize the basic Boolean logic functions AND, OR, NAND, NOR, and the Majority operation.[9,10,19]

However, despite the reprogrammable gates and implication gates being good examples for the realization of stateful logic, there are still some shortcomings that need to be addressed. In the aspect of device performance, the STT-MTJ suffers from serious failure and reliability issues due to the high writing current densities as well as erroneous writing by the read current.[20] Furthermore, both the single implication gate and the single reprogrammable gate can only implement just one or a limited number of logic operations, indicating more steps and complex combinations are needed to complement the other basic Boolean logic functions. Therefore, it is extremely attractive to explore a better alternative to the STT-MTJ and to finally realize as many Boolean logic functions as possible in such a single device.

Spin–orbit torque (SOT) originating from the spin Hall effect and Rashba–Edelstein effect provides another method to realize magnetization switching[21–23] and high-speed domain wall motion[24,25] by an in-plane current injection. Moreover, the critical current of the SOT-induced switching can be modulated with a bias voltage due to the voltage-controlled magnetic anisotropy (VCMA) effect,[26,27] exhibiting great potential in the application of MTJ-based logic devices.

In this work, a design based on the SOT mechanism was experimentally demonstrated to realize all 16 Boolean logic functions in a simple Ta/CoFeB/MgO trilayer with perpendicular magnetic anisotropy (PMA). The key idea is to combine different logic inputs to tune the magnetization state and to measure the anomalous Hall resistance as the logic output. Furthermore, by utilizing the tunnel magnetoresistance (TMR) value as the logic output, this method is applicable to the emerging perpendicular SOT-MTJ, a novel three-terminal device with high reliability, symmetric switching, and scalable energy consumption compared to the conventional STT-MTJ. More importantly, we also conceive that by combing the voltage-controlled magnetic anisotropy (VCMA) effect, the modified method (using current injection and bias voltage as logic inputs) can realize all 16 Boolean logic functions in the SOT-MTJ.

The multilayers with a core structure of Ta (3)/$Co_{40}Fe_{40}B_{20}$ (1.1)/MgO (2)/Ta (3) (in nm) were deposited on thermally oxidized Si (001) substrates by a magnetron sputtering system at room temperature. The films were patterned into 15-μm-wide Hall bars for transport measurements using photolithography and Ar-ion etching. The devices exhibit PMA after an annealing process at above 300 °C, which can be proved by the anomalous Hall signal with an out-of-plane magnetic field (Fig. S1, supplementary material). Figure 1(a) shows SOT-induced magnetization switching, with current injection (I_x) and magnetic field (H_x) both along the x-axis. Opposite switching can be clearly observed when H_x is reversed, suggesting similar features to the previous studies on perpendicularly magnetized heavy metal/ferromagnet heterostructures.[21,28] Figure 1(b) presents current-induced switching loops under different H_x, indicating that the critical switching current is positively correlated with H_x, which can be explained by the Marco model.[29] Moreover, programmable logic devices based on the SOT mechanism can be designed according to this relationship.

Figure 2(a) shows two schematic current-induced switching loops under different external fields in consideration of a single domain switching paradigm. The critical switching currents can be distinguished in the high external field (H_H) and low external field (H_L) configurations. Hence, a median value of two critical switching currents is defined as $|I_M|$. Similar to the schematic curves, distinctly different switching loops corresponding to different external fields can be observed in the experimental measurements, as shown in Fig. 2(b). Here, H_H and H_L are 200 Oe and 30 Oe, respectively, and the value of $|I_M|$ is 8.5 mA. The external field H_x and injected current I_x are used as two input variables to perform logic operations. For example, H_x is 30 Oe or 200 Oe for input 0 or 1, respectively, and I_x is set to −8.5 mA or +8.5 mA for input 0 or 1, as listed in the table in Fig. 2(c). The measured Hall resistance functions as the logic output, which can be identified as the spin-up state (logic "1") and the spin-down state (logic "0"), as shown in Fig. 2(c). Figure 2(d) suggests the logic output transformation corresponding to different logic inputs (external field/current, H_xI_x). It can be seen from the diagram that for the H_xI_x = "11" configuration (H_x = 200 Oe and I_x = +8.5 mA), the logic output is 1 (spin-up state), regardless of the initial magnetization state. Similarly, the H_xI_x = "10" configuration leads to the logic output 0, and SOT-induced switching will not take place with the logic input H_xI_x = "00" or "01" configuration. Based on these working principles, all 16 Boolean logic operations can be performed, and the detailed operations are listed in Fig. 2(e).

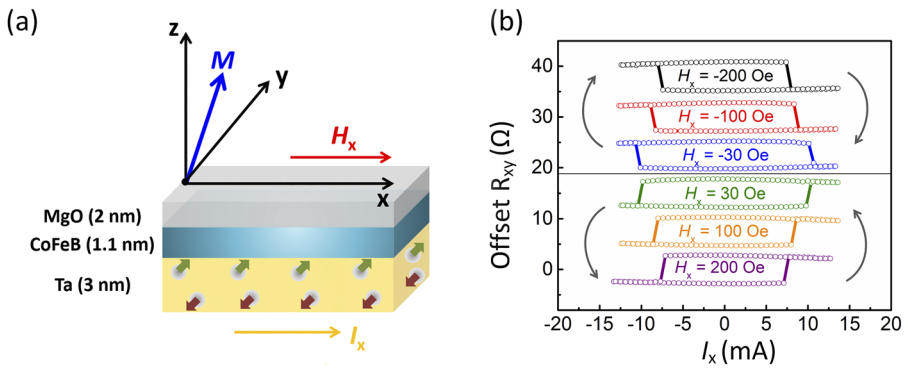
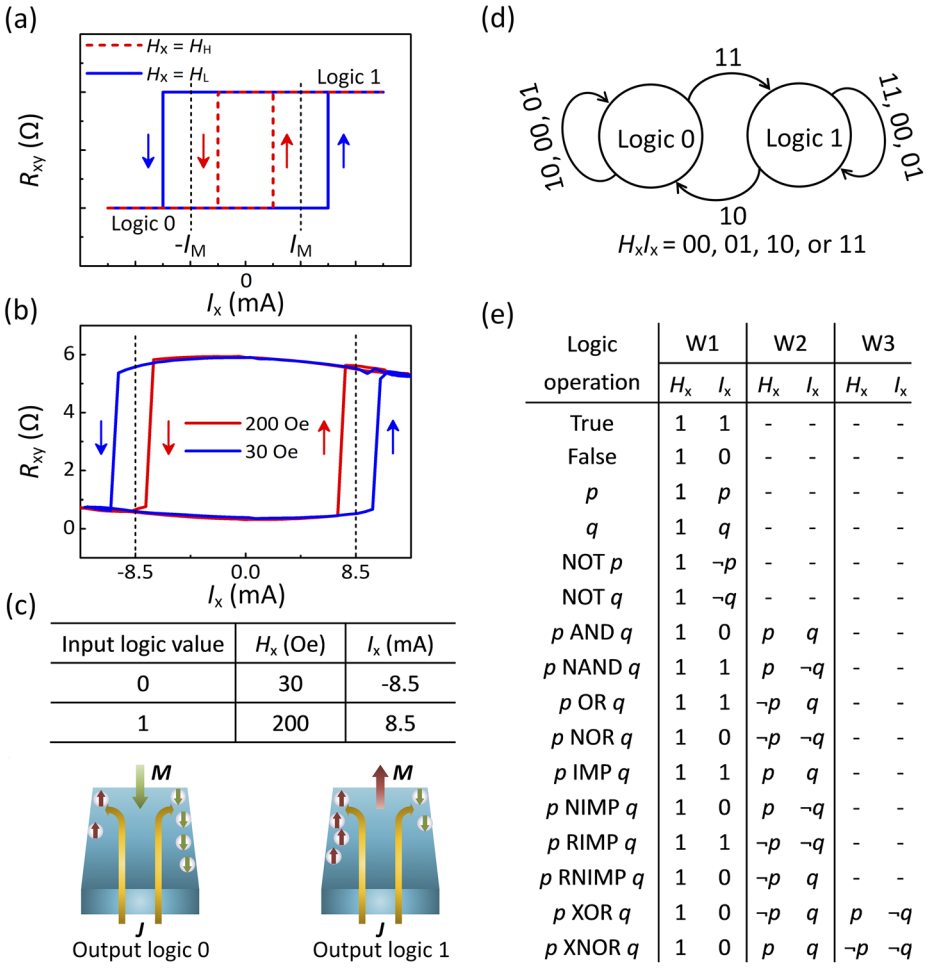


FIG. 1. (a) Illustration of a Ta/CoFeB/MgO Hall bar device. H_x and I_x refer to in-plane field and current injection along the x axis, respectively. (b) Current switching loops under different H_x (the arrows shown in the figure indicate the switching polarities of the SOT-induced switching).



(c)

Input logic value	H_x (Oe)	I_x (mA)
0	30	-8.5
1	200	8.5

(e)

Logic operation	W1		W2		W3	
	H_x	I_x	H_x	I_x	H_x	I_x
True	1	1	-	-	-	-
False	1	0	-	-	-	-
p	1	p	-	-	-	-
q	1	q	-	-	-	-
NOT p	1	$\neg p$	-	-	-	-
NOT q	1	$\neg q$	-	-	-	-
p AND q	1	0	p	q	-	-
p NAND q	1	1	p	$\neg q$	-	-
p OR q	1	1	$\neg p$	q	-	-
p NOR q	1	0	$\neg p$	$\neg q$	-	-
p IMP q	1	1	p	q	-	-
p NIMP q	1	0	p	$\neg q$	-	-
p RIMP q	1	1	$\neg p$	$\neg q$	-	-
p RNIMP q	1	0	$\neg p$	q	-	-
p XOR q	1	0	$\neg p$	q	p	$\neg q$
p XNOR q	1	0	p	q	$\neg p$	$\neg q$

FIG. 2. (a) Schematic switching loops under high external field (H_H) and low external field (H_L); the median value of two critical switching currents is defined as $|I_M|$. (b) Corresponding experimental switching loops under 200 Oe (H_H) and 30 Oe (H_L), where $|I_M|$ is 8.5 mA. (c) The correspondence between input logic values and H_x as well as I_x. The illustration suggests the output logic values corresponding to magnetization states. (d) Transition of the output logic states by H_xI_x combined operations. (e) Detailed operation methods of all 16 Boolean logic functions (W1, W2, and W3 stand for a write sequence).

Therefore, "p" and "q" are the two input logic variables, "-" means no operation, and "¬" represents the negation operation, i.e., ¬0 = 1 and ¬1 = 0.

Figure 3 shows the experimental results of Boolean logic functions based on the SOT-induced switching. Combining with a truth table of all 16 Boolean logic gates (shown in supplementary material), the feasibility of complementary logic operation in a single device with programmability and non-volatility can be demonstrated. For example, a TRUE gate can be performed in one step with the logic operation "11" (H_x = 200 Oe and I_x = +8.5 mA), regardless of the value of inputs p and q. For this configuration, the final magnetization is in the spin-up state, outputting a logic value 1, as shown in Fig. 3(a1). For an AND gate, if the input $p = q = 0$, a logic operation H_xI_x = "10" (H_x = 200 Oe and I_x = −8.5 mA) is needed as an initialization step. Then, the writing operation "00" is performed by H_x = 30 Oe and I_x = −8.5 mA. In this case, the final magnetization state is "spin-down," outputting a logic value 0, as shown in Fig. 3(b1). For the configurations with other "p q" values, "01," "10," and "11," the logic function can be realized by writing "p q" after an initialization step with "10," outputting the corresponding results finally, as shown in Figs. 3(b2)–3(b4). For an OR gate, the logic input I_xH_x = "11" (H_x = 200 Oe, I_x = +8.5 mA) is initially operated if the input $p = 1$ and $q = 0$. Then, the write operation "¬p q" ("00," H_x = 30 Oe, and I_x = −8.5 mA) is performed as the second step, resulting in the spin-up state (output 0), as shown in Fig. 3(b5). For configurations with other "p q" values, "11," "00," and "01," the logic operations can be completed by writing "¬p q" after an initialization step with "11," and the corresponding experimental results are shown in Figs. 3(b6)–3(b8).

Moreover, an XOR gate can be realized in a process with three steps. If the logic input $p = 0$ and $q = 1$, the write operation H_xI_x = "10" (H_x = 200 Oe and I_x = −8.5 mA) is performed at first. The second step is to input "¬p q" ("11," H_x = 200 Oe, and I_x = +8.5 mA). Write operation "p ¬q" ("00," H_x = 30 Oe, and I_x = −8.5 mA) is performed at last. After the three-step operations, the final magnetization state is spin-up, outputting a logic value 1, as shown in Fig. 3(c4). As for the other "p q" values of "10," "11," and "00," the initial operation is to input "10" and then input "¬p q" as follows. The third step is to perform a logic operation "p ¬q" and read the corresponding output values finally. The relevant experimental results are shown in Figs. 3(c1)–3(c3). In addition, the operations of other logic gates not mentioned here are

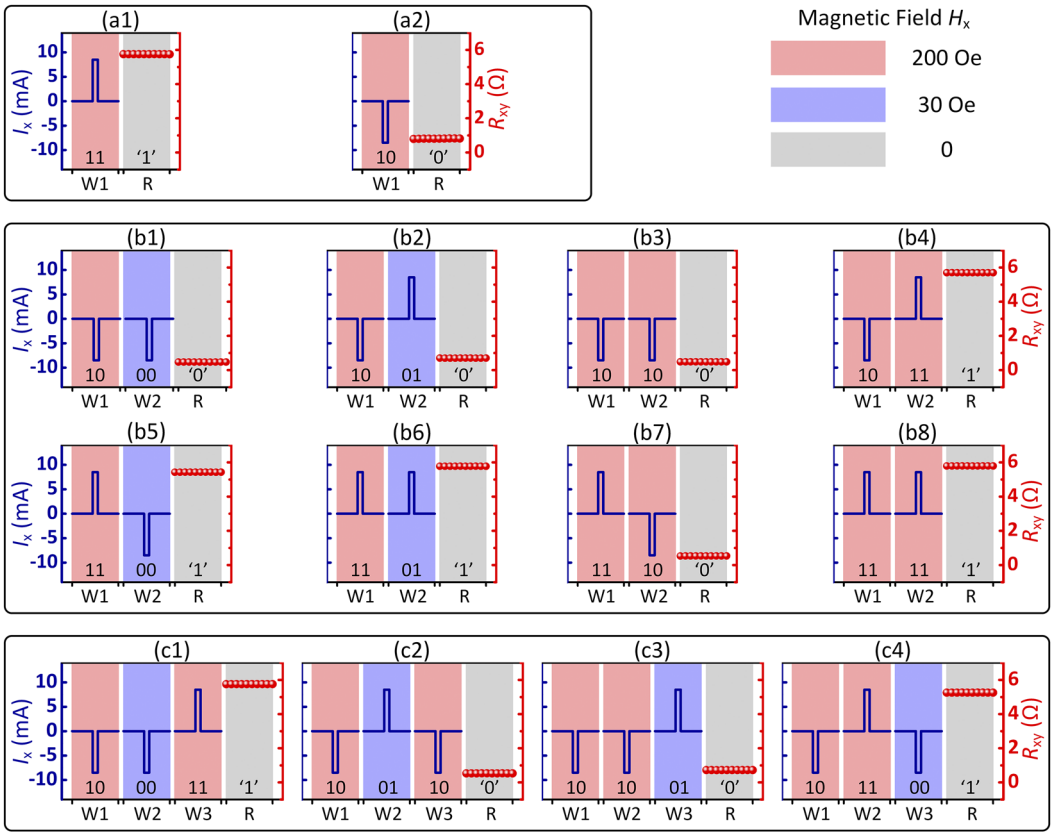


FIG. 3. Experimental results of all 16 Boolean logic functions based on the SOT switching mechanism. (a)–(c) represent the realization of logic functions by using one, two, and three write cycles, respectively.

summarized in the truth table (Fig. S2, supplementary material). It clearly indicates that these experimental results demonstrate the feasibility to successfully realize all 16 Boolean logic operations in the Ta/CoFeB/MgO device. It means that the SOT-based logic operations can be introduced into the device design, which is expected to realize the combination of non-volatile memory and computing unit in an integrated circuit, breaking the von Neumann bottleneck in the future.

Furthermore, the external field can be replaced by bias voltage as a logic input based on the VCMA effect.[30,31] As shown in Fig. 4(a), charge accumulation will take place at the ferromagnetic metal/oxide interface in the MTJ structure with a bias voltage (V_b) applied. The energy barrier of magnetization switching is thus modulated due to the change in the relative occupancy of the *3d*-orbitals.[32] Figure 4(b) shows the specific influence of the bias voltage on the energy barrier of magnetization switching in the free layer, suggesting a lower barrier corresponding to a positive bias voltage and a higher barrier corresponding to a negative bias voltage. The voltage required to completely eliminate the barrier is defined as V_c. The voltage-driven switching induced by SOT can be realized by precisely controlling the duration of the bias voltage when $0 < V_b < V_c$.[32,33] Based on this feature, a VCMA-assisted SOT MTJ device was designed, as shown in Fig. 4(c). A low energy barrier is achieved with a bias voltage applied between terminals T1 and T3, and the SOT originated from the heavy metal layer is induced by an injected current between T2 and T3 that results in a current-induced switching. This procession can be described by the Landau–Lifshitz–Gilbert (LLG) equation,[34]

$$\frac{d\vec{M}}{dt} = -\gamma\vec{M} \times \vec{H}_{eff} + \alpha\vec{M} \times \frac{d\vec{M}}{dt} + \vec{\Gamma}, \tag{1}$$

where $\vec{M}$ is the magnetization vector, γ is the gyromagnetic ratio, and α is the Gilbert damping coefficient. The effective magnetic field $H_{eff} = H_{ext} + H_d + H_{ani}$ is the sum of the external field (H_{ext}), the demagnetizing field (H_d), and the anisotropy field (H_{ani}). Taking into account the VCMA effect, H_{ani} can be expressed in the form[33]

$$\vec{H}_{ani(V_b)} = \left(\frac{2K_{i(0)}t_{ox} - 2\xi V_b}{M_s t_f t_{ox}}\right)\vec{M}, \tag{2}$$

where $K_{i(0)}$ is the interfacial anisotropy energy without bias voltage applied, t_{ox} and t_f are the thickness of the barrier and the free layer, respectively, ξ is the VCMA coefficient, and M_s is the saturation magnetization of the free layer. The additional SOT item in

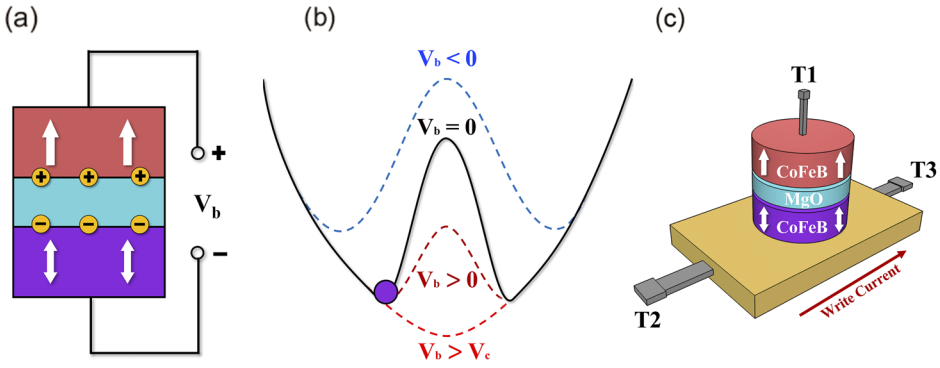


FIG. 4. Illustrations of (a) MTJ structure, (b) impact of different voltages on the energy barrier of an MTJ, and (c) the VCMA-assisted SOT MTJ device.

the LLG equation can be described as

$$\vec{\Gamma} = -\frac{\gamma\hbar\theta_{SHE}J}{2et_fM_s}\vec{M}\times\left(\vec{M}\times\vec{\sigma}\right), \tag{3}$$

where θ_{SHE} is the spin Hall angle and $\vec{\sigma}$ is the spin polarization vector. Hence, the dynamic evolution of the magnetization in the free layer can be characterized according to Eqs. (1) and (3). Based on this, Verilog-A language was applied to build electrical models for a VCMA-assisted SOT MTJ device to perform numerical simulations with a 40-nm CMOS kit.[33] The detailed parameters for the model can be found in Table S3 listed in the supplementary material. The simulation results suggest that all 16 Boolean logic functions can be realized based on the VCMA and SOT effects. Figure 5 shows the transient waveforms of the proposed VCMA-assisted SOT MTJ device corresponding to AND, OR, and XOR logic gates.

Bias voltage V_b and injected current I_x are used as two input variables to perform logic operations. V_b is set as 0 mV or 600 mV for input 0 or 1, respectively, and I_x is set to $-65\ \mu A$ or $+65\ \mu A$ for input 0 or 1, respectively. The application of bias

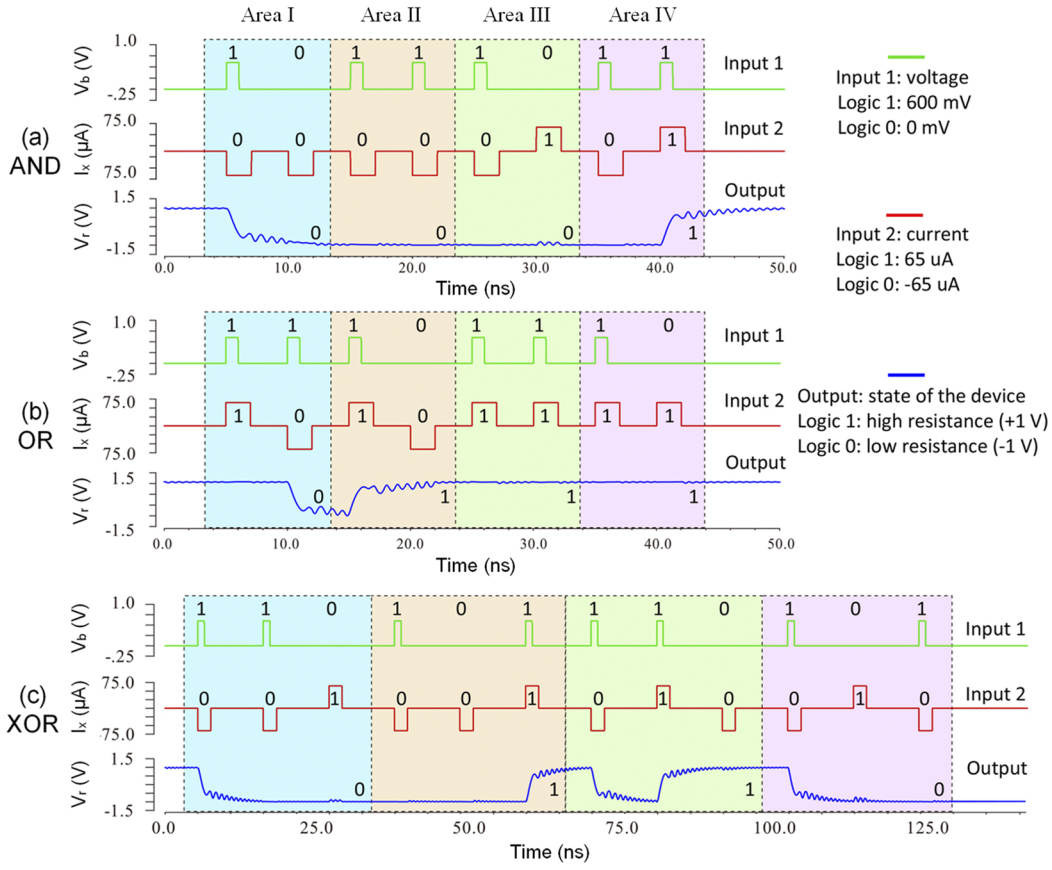


FIG. 5. Transient waveforms of the proposed VCMA-assisted SOT MTJ device corresponding to (a) AND, (b) OR, and (c) XOR logic gates.

voltage can lead to a lower energy barrier, and the SOT is generated by the injected current, resulting in a switching of the magnetization state of the free layer in the device. The logic output is defined based on the tunneling magnetoresistance (TMR) corresponding to the anti-parallel state (high resistance, +1 V, logic 1) or parallel state (low resistance, −1 V, logic 0) of the two ferromagnetic layers. The transient waveforms of each logic operation shown in Fig. 5 are divided into four color areas (areas I-IV), representing the operation process when the initial logic input "p q" = "00," "10," "01," and "11," respectively. For an AND gate shown in Fig. 5(a), if the inputs $p = q = 0$ (area I), the initialization step is to perform a logic operation "10," setting the bias voltage to 600 mV (1 ns) with a pulsed injected current of $-65\ \mu A$ (2 ns). Then, the logic operation "00" is performed by $I_x = -65\ \mu A$ without bias voltage applied. The device is in the low-resistance state finally in this case, outputting a logic value 0. For the configurations with other "p q" values, "10" (area II), "01" (area III), and "11" (area IV), the logic operation can be completed by writing "p q" after an initialization step with "10" and outputting the corresponding results. For an OR gate shown in Fig. 5(b), if the inputs $p = 1$ and $q = 0$ (area II), a write operation "11" (V_b = 600 mV and $I_x = +65\ \mu A$) is performed at first. Then, the operation is completed by a write operation "$\neg p$ q" ("00," V_b = 0 mV, and $I_x = -65\ \mu A$) that results in a high-resistance state (1 V, output 1). For configurations with other "p q" values, "00" (area I), "01" (area III), and "11" (Area IV), the logic operation can be completed by writing "$\neg p$ q" after an initialization step with "11," similar to the discussion above. Figure 5(c) shows the realization of an XOR gate with three steps. If the logic input $p = 0$ and $q = 1$ (area III), the write operation "10" (V_b = 600 mV and $I_x = -65\ \mu A$) is performed at first, leading to the low-resistance state. The second step is to input "$\neg p$ q" ("11," V_b = 600 mV, and $I_x = +65\ \mu A$), and write operation "p $\neg q$" ("00," V_b = 0 mV, and $I_x = -65\ \mu A$) is performed at last. Finally, the device is in the high-resistance state outputting a logic value 1 after the three-step operations. As for the other input values of "p q," "00" (area I), "10" (area II), and "11" (Area IV), the logic function can be performed with three operations of input "10," "$\neg p$ q," and "p $\neg q$," reading the corresponding logic output value finally. Based on this, a VCMA-SOT assisted MTJ device with three terminals is designed, and the feasibility of realizing all 16 Boolean logic functions in a single unit is demonstrated. The simulation results suggest that the operation with a single step only needs 2.26 ns, featuring an ultra-fast writing speed.

In summary, all 16 Boolean logic functions in a single Ta/CoFeB/MgO device with PMA were experimentally demonstrated based on the SOT effect by applying the external field and current injection as input variables. Furthermore, the VCMA effect was introduced to design a three-terminal MTJ device, which can implement magnetic field-independent logic operations. The approach can be improved through optimization of structure design and device fabrication, paving the way for the application of energy efficient spin-based logic, which is beyond the current von Neumann computing architecture.

SUPPLEMENTARY MATERIAL

See the supplementary material for the anomalous Hall signal of the device, the truth table of all 16 Boolean logic functions, and the detailed parameters for the electrical model to perform numerical simulations.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon request.

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