SCIENCE CHINA
Technological Sciences

•Article•

https://doi.org/10.1007/s11431-021-1980-1

# Semi-custom methodology to fabricate transmission electron microscopy chip for *in situ* characterization of nanodevices and nanomaterials

YU BoCheng[1], SUN Mei[2], PAN RuHao[3], TIAN JiaMin[4], ZHENG FengYi[1], HUANG Dong[1], LYU FengJiao[4], ZHANG ZhiTong[1], LI JunJie[3], CHEN Qing[4] & LI ZhiHong[1*]

[1] *National Key Laboratory of Nano/Micro Fabrication Technology, School of Integrated Circuits, Peking University, Beijing 100871, China;*
[2] *Hefei National Laboratory for Physical Sciences at the Microscale, University of Science and Technology of China, Hefei 230026, China;*
[3] *Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing 100190, China;*
[4] *Key Laboratory for Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China*

Received July 21, 2021; accepted December 9, 2021; published online March 10, 2022

The fabrication of nanodevices on the delicate membrane window of the TEM (transmission electron microscopy) chip has the risk of breakage failure, limiting in-depth research in this area. This work proposed a methodology to address this issue, enabling secure *in-situ* transmission electron microscopic observation of many devices and materials that would otherwise be difficult to achieve. Combining semi-custom TEM chip design and front-side protected release technology, a variety of nanodevices were successfully fabricated onto the window membrane of the TEM chip and studied *in situ*. Moreover, the pressure tolerance of window membrane was investigated and enhanced with a reinforcing structure. As an example of typical applications, $MoS_2$ devices on the TEM chip have been fabricated and electron beam-induced gate modulation and irradiation damage effects, have been demonstrated.

***in situ* TEM, TEM chip, nanodevice, membrane window, nanomaterial**

**Citation:** Yu B C, Sun M, Pan R H, et al. Semi-custom methodology to fabricate transmission electron microscopy chip for *in situ* characterization of nanodevices and nanomaterials. Sci China Tech Sci, 2022, 65, https://doi.org/10.1007/s11431-021-1980-1

## 1 Introduction

Transmission electron microscopy (TEM) is a powerful tool for characterizing structural and chemical properties. In recent years, *in situ* TEM study of materials in different ambient, temperature, and bias conditions has shown a significant role in the fields of catalysis, energy, and device mechanism [1–10]. Following the probe approach, the method using TEM chips was designed and manufactured to achieve various *in situ* functions. The TEM chip has become a key technology because its membrane window can carry out gas/liquid environment experiments, load nanodevices, and has the advantages of small size, low cost, and the possibility to expand into a wide range of electrically achievable functions [11–18].

The observing window area of the TEM chip is a suspended thin and fragile membrane. It is a challenging and tricky task to prepare nanodevices and nanomaterials on such a membrane. Most reported methods of sample preparation are evaluated in Table 1 [19–40]. In the most classic way, the chips with the released membrane can be purchased from manufacturers or fabricated by the end-users themselves. Then the nanomaterials or nanodevices are carefully prepared on the suspended membrane. However, the procedure highly risks damaging membrane, and only allows limited and gentle processes [19–33]. Another approach is to prepare

*Corresponding author (email: zhhli@pku.edu.cn)

**Table 1** Risk of damaging membrane, sample, and chip edges for different TEM chip preparing methods

| Fabrication order | Sample transfer method | Membrane release method | Risk of damaging | | | Proficiency requirement | Refs. |
|---|---|---|---|---|---|---|---|
| | | | Membrane | Sample | Chip edge | | |
| Release membrane before preparing sample | Deposition | Released | Low | Low | Low | Low | [19,20] |
| | Contact | | High | Low | Low | Medium | [21] |
| | Stamp | | Medium | High | Low | High | [22,23] |
| | Nano-manipulation | | Medium | Low | Low | High | [24–28] |
| | Liquid surface | | Medium | Low | Low | High | [29] |
| | Sample solution droplet | | Low | Medium | Low | Low | [30–33] |
| Release membrane after preparing sample | Transferred | Protective layer | Medium | High | Medium | Low | [34–36] |
| | | Sealing ring | Low | Medium | Medium | High | [37] |
| | | Floating chip | Low | Medium | High | High | [38,39] |
| | | Epoxy seal | Low | Medium | High | High | [40] |
| | | Etching apparatus | Low | Low | Low | Low | This work |

the sample on a chip with the unreleased membrane using an unlimited transfer process, and then etch the silicon to release the window membrane. The currently reported methods may still have problems such as contamination of samples, poor feasibility to diced chips, or require high proficiency [34–40].

To pursue the highest success rate to release the membrane, the approach of utilizing an optimized etching apparatus is a preferential choice. The most available etching apparatuses are unsuitable for etching small areas on small chips. The size of the individual TEM chip is much smaller than the conventional wafer size, which can cause clamping difficulty. At the same time, the tiny etching area will prevent the effective flow of the etchant, thus causing unstable etch.

For many applications, the larger the window, the greater the probability of having the desired sample on the window. However, the large window is more prone to break during both fabrication and usage in TEM. Therefore, prediction and enhancement of the suspended membrane become valuable in chip design and fabrication.

In this paper, we propose a semi-custom fabrication method, which uses an optimized etching apparatus for post-transfer membrane release, therefore allowing the preparation of complex nanodevices on the membrane with a high yield. We provide a complete and comprehensive process with detailed recipes and design rules, which are applicable to achieve *in situ* characterization of various nanostructured samples. In addition, the pressure resistance of the membrane is also optimized with the reinforcing structure. Finally, we show four *in situ* TEM experiments of nanodevices prepared by our method, which are difficult to prepare equivalently using other methods. Among them, we perform an in-depth *in situ* TEM study of the electrical response to electron beam irradiation of $MoS_2$ nanodevices.

## 2 Experiments and analysis

### 2.1 Fabrication methodology

As illustrated in Figure 1(a), a TEM chip is expected to be a platform for TEM observing and performing *in situ* studies for a wide range of devices and materials. However, for chips with released membranes, adding devices or materials on top of them is risky as it tends to cause membrane rupture. When the membrane is supported with silicon underneath, as shown in Figure 1(c), it can host a variety of processes, including press-on material transfer, blade coating, ultrasound, etc. It is initially versatile for nanodevices and nanomaterials characterization and can then be customized according to the demand afterward, so given the name of semi-custom TEM chip.

The fabrication process of the chip is shown in Figure 2. The high-quality low-stress silicon nitride ($SiN_x$) layer is grown on a 200-μm-thick silicon wafer with low-pressure chemical vapor deposition (LPCVD). The membrane thickness is less than 100 nm, typically 50 nm. Then photolithography and reactive ion etching (RIE) are used to form the window pattern on the backside. This step requires precise alignment mask-crystal direction to make window size accurate (Figure 2(b)). Next, after double-sided alignment photolithography, metal sputtering, and lift-off process, the metal electrodes are fabricated. A protection layer is then patterned on the top (Figure 2(c)). The wafer is later diced into single chips with size fitting the TEM holder.

As shown in Figure 2(d), there are uncovered leads on the chip for further connection onto devices, and the chip has marks for aligning. There are also large numbers or patterns on the corner of the chip, displaying information of chip design that is visible to bare eyes. Here, the semi-custom chips can be produced in large quantities and the cost per chip is reduced.

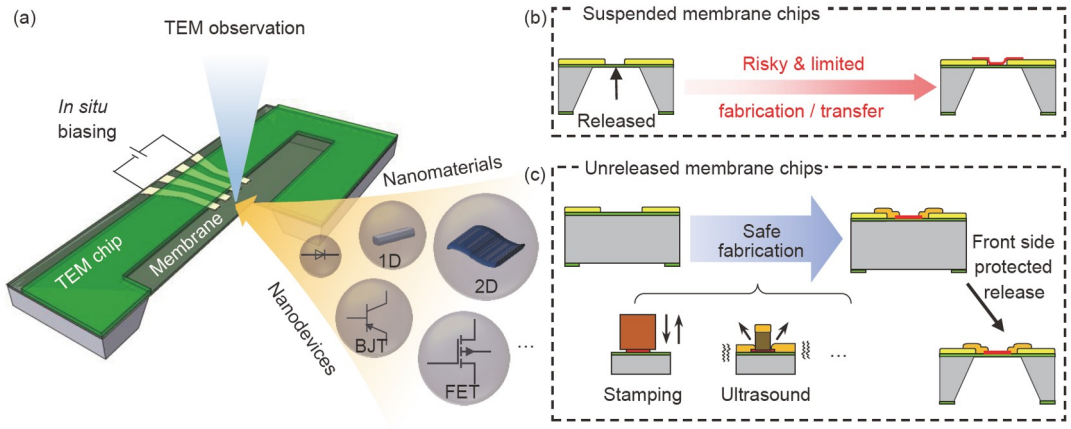


**Figure 1** (a) The idea of TEM chip as a platform for nanodevices and nanomaterials in the *in situ* TEM research; (b) the schematic diagram of adding nanomaterial on the suspended membrane chips; (c) the schematic diagram of the fabrication of nanodevice on unreleased membrane chips.

According to the subsequent customized demand, nanodevice processing is performed on the unreleased membrane chip, which generally contains hard contact material transfer, electron beam photolithography, and ultrasonic material removal. After that, the chip needs a special front-side protected selective etching to etch silicon and release the membrane (Figure 2(f)). The obtained chips are ready for *in situ* TEM characterization as shown in Figure 2(g) and (h).

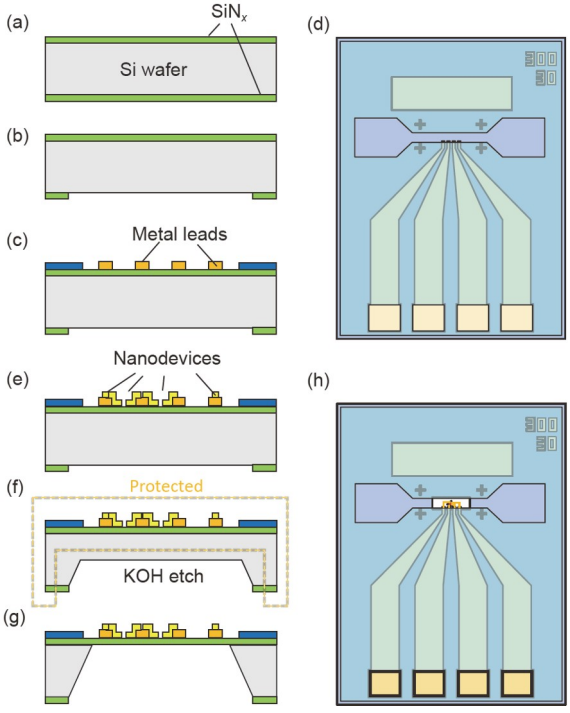


**Figure 2** Fabrication procedure for the chip with nanodevices on the silicon nitride window membrane. (a)–(c) The side view and (d) the top view of the chip at step (c). (e)–(g) The side view and (h) the top view of the fabrication process of adding nanodevices onto the chip membrane window in preparation for *in situ* TEM observation.

## 2.2 Etching setups

The conventional etching methods need a protective layer on the device area, which is removed after etching. There are two requirements for the protective layer process: (1) the protective layer should be invulnerable to the strong etchants during the long etching process, and (2) the final suspended membrane and nanomaterials should be invulnerable to solvents and operations for removal of the protective layer. Obviously, the contradiction between the two requirements makes it inapplicable.

We designed and optimized a special etching apparatus as shown in Figure 3(a) to hold the etchant in place so it only contacts a selected area. The etching apparatus consists of a Teflon container, a heater, a stainless-steel holder, etc. The 30wt% KOH is used to anisotropically etch the exposed silicon under the window area at 80°C. A magnetic rotor is utilized to stir the etchant magnetically, so the air bubbles generated during the reaction can be quickly separated from the surface, to avoid the micro-mask effect to achieve good corrosion uniformity. At the same time, the window area remains untouched throughout the membrane release process. Another advantage of the technique is that the etch-stop can be conveniently monitored from the top of the apparatus which helps prevent further damage to the fragile membrane after the etching of the silicon. As the silicon etching nears completion, the window will become transparent and light from a light source below the device will be observable from the top of the apparatus.

As shown in Figure 3(c) and (d), the apparatus ensures a high efficiency because it can etch up to 8 chips simultaneously. The chips are loaded into the grooves where the etching area will face holes on the Teflon container. These grooves prevent chips from slipping or cracking while reducing operational difficulty and error rates. The corrosion-resistant fluoroelastomer O-ring used in the device has ex-

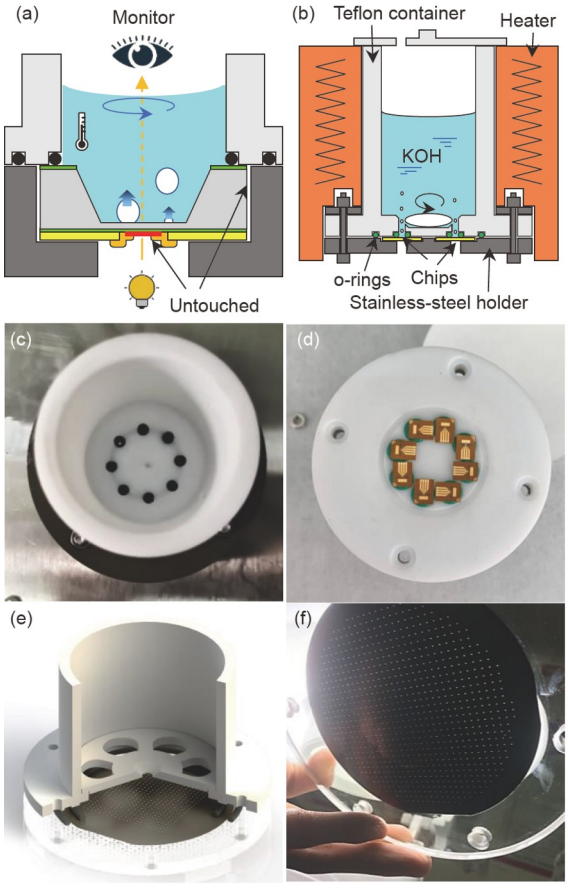


**Figure 3** (a) The schematic diagram of the implementation of the front side protected releasing; (b) the schematic diagram of the etching apparatus; (c) the view from the top of Teflon container after etching; (d) chips after etching; (e) the apparatus for whole wafer etching with a similar design; (f) the whole wafer etching result.

cellent uniformity, and the metal ring on the upper part of the device and the metal bracket on the lower part of the device have high hardness and flatness so that each chip can be tightened uniformly by using a fixed-torque screwdriver and tightening the four screws in sequence from low to high torque. After the disassembly of the etching device, the chips are all face up in a position where can be easily and reliably clamped.

The design principle of this etching apparatus can be extended to other sizes, such as the case of single-sided etching scenarios of the entire four-inch silicon wafer, as illustrated in Figure 3(e) and (f).

### 2.3 Membrane strength reinforcing structure

Most TEM chips based on silicon wafers use anisotropic etching to make rectangular windows, releasing the suspended $SiN_x$ membrane as the observing window. In order to increase the membrane stability, we have investigated many methods and found that introducing a reinforcing structure grown on the $SiN_x$ membrane is the best. Using the parameters of window size 300 μm × 50 μm, and membrane thickness 50 nm into the simulation, stress distribution result of the membrane without (Figure 4(b)) and with reinforcing structure (Figure 4(c)) are shown. A clearer stress data comparison in Figure 4(d) and (e) show the reinforcing structurehas effectively reduced the maximum stress. According to Weibull distribution, it reduces the fracture possibility [41,42]. The result points out that two places need caution. The place ② is on the surface of $SiN_x$ membrane, at the inner edge of the unreinforced part. The place ③ is on the surface of the reinforcing structure, directly above the edge of silicon.

To analyze the change in tensile stress, we need to consider how the forces change for different reinforced layer thicknesses ($t_{rs}$) and reinforcing structure length ($L_{rs}$).

The total tensile stress on the membrane is fixed for a certain size window under a fixed pressure difference. The maximum tensile stress at place ② is related to the bending angle of the $SiN_x$ membrane. As shown in Figure 4(f), the stress is reduced only when the reinforcing structure is thin and long.

At the top of the reinforced membrane, the maximum stress will be less if the membrane is thicker. The result of the simulation in Figure 4(e) is consistent with this analysis. One thing to note is that the material at place ③ is different, meaning that the stress endurance ability is different. This reinforced membrane is often formed by sputtering or plasma-enhanced chemical vapor deposition (PECVD) process so their fracture strength is often lower than the $SiN_x$.

The stresses at both places ② and ③ need to be reduced to ensure that the reinforcing structure is one that reduces the probability of the fracture. A structure with an extended width of >3 μm and thickness of >100 nm can achieve good membrane strength reinforce.

When the window size or the pressure difference is larger, a frame-like reinforcing structure is not enough. Longitudinal and latitudinal stiffener structures can provide stronger reinforcement and lower the maximum stress on the thin membrane. The stiffener structure requires a high mechanical strength of its material and also requires a thickness of several hundred nanometers. After comprehensive consideration, LPCVD grown $SiO_2$ is the best choice. As demonstrated in Figure 4(h), when a $SiO_2$ stiffener structure is placed on the membrane surface of a 300 μm×300 μm TEM window, the stress is reduced to an acceptable value.

## 3 Results and discussion

### 3.1 Pressure test for window membrane

Since it is difficult to test the chip pressure resistance in an electron microscope, we design a device to compare and measure the chip pressure resistance. As shown in Figure 5(a), two types of chips with and without a reinforcing structure

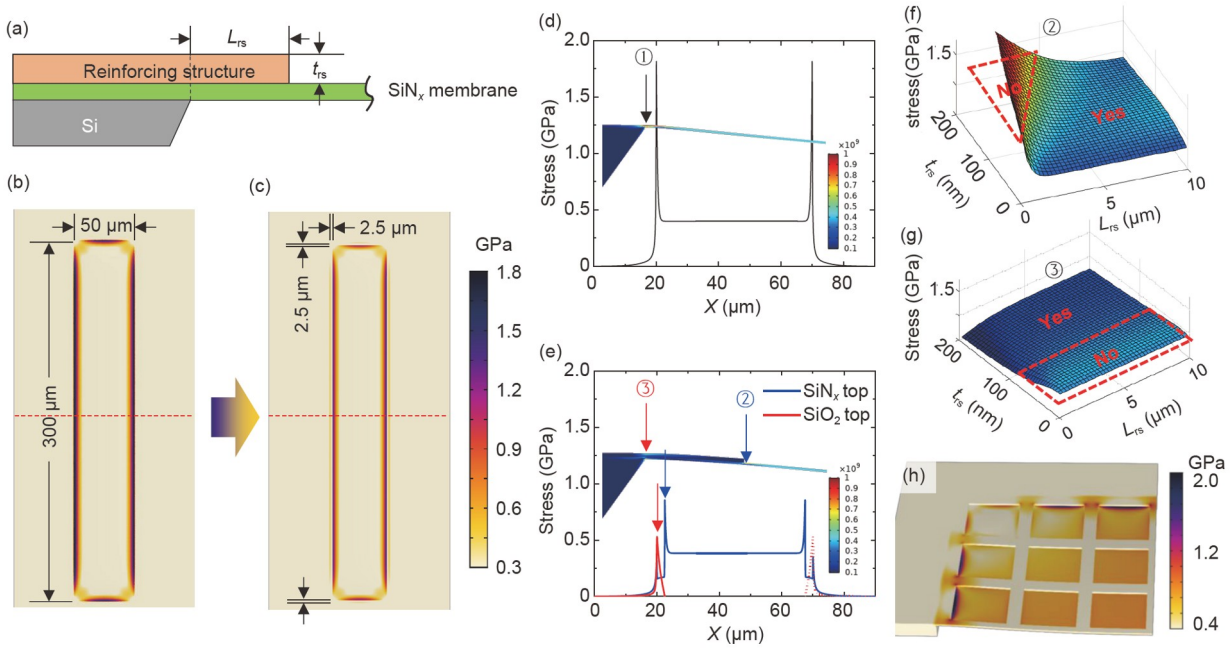


**Figure 4** Simulation results of stress on membranes. (a) The schematic diagram of the membrane and the reinforcing structure at the edge of the window. (b) The simulated stress distribution on 300 μm×50 μm size 50 nm $SiN_x$ membrane under a pressure difference of standard atmospheric pressure. (c) The stress distribution with a 2.5 μm $SiO_2$ reinforcing structure. (d) The surface stress distribution and the side view of the structure at the edge of the membrane without or (e) with the reinforcing structure. (f) The maximum stress on the $SiN_x$ membrane at different thicknesses and lengths of the reinforcing structure. The "No" region shows the parameters easier membrane break. (g) The maximum stress on the top of reinforcing structure. (h) The simulation result of the stress on a 300 μm×300 μm window with stiffener structure.

can be tested under the conditions of the same air pressure source. A 3-bar nitrogen source is repeatedly added as pressure difference input.

Two kinds of chips are fabricated in the same process, among which one extended the spacer structure as reinforcing structure. $TaO_x$ is chosen as the material instead of $SiO_2$ to compare the membrane strength with or without the reinforcing structure. It is an insulating material prepared by sputtering, and the sputtering-prepared material does not require etching removal and thus damage to the substrate $SiN_x$ material. The previous analysis reveals that the reinforcing structure needs a relatively large thickness. A group of chips with 120 nm material thickness is tested for comparison. The nitrogen fractured the unreinforced membrane window but failed to break the reinforced one, proving the effectiveness of the reinforcing structure.

### 3.2 Large window and stiffener structure

Sometimes a larger observation window of the TEM chip becomes necessary to allow more nanomaterials in the observation area under the same conditions. Moreover, a larger observation window may simply be required because the object to be observed needs a larger window to carry. In the situation that the TEM chip with a larger window membrane demands more careful protection, our applicable methodology gains more advantages.

Utilizing the $SiO_2$ stiffener structure analyzed above, a $SiN_x$ membrane window with a thickness of 50-nm-thick size of 300 μm×300 μm is designed on the TEM chip. The ZnO nanowire is transferred onto the window area of the unreleased chip with front-side protected releasing and observed in TEM. Figure 6 shows that this design provides a large window with enough load capacity to be applied with sufficient clarity.

### 3.3 Nanodevices and *in situ* TEM study

Following such a post-release device processing method, a wide variety of nanodevices can be reliably fabricated. Figure 7 shows the fabricated membrane-released semi-custom TEM chip.

The various nanodevices fabricated using the semi-custom chip method are shown in Figure 8.

A graphene nanogap device is shown in Figure 8(a) and (b). The sub-10 nm nanogap is prepared by the shadow deposition method [43,44] after the transfer of single layer graphene utilizing liquid surface onto the unreleased chip. Among these fabrication steps, all transferring graphene, electron beam lithography (EBL), and metal lift-off possibly cause damages if the membrane is previously released. Also, graphene devices are very reluctant to various organic contamination. Using our post-release method can achieve reliable device assemble.

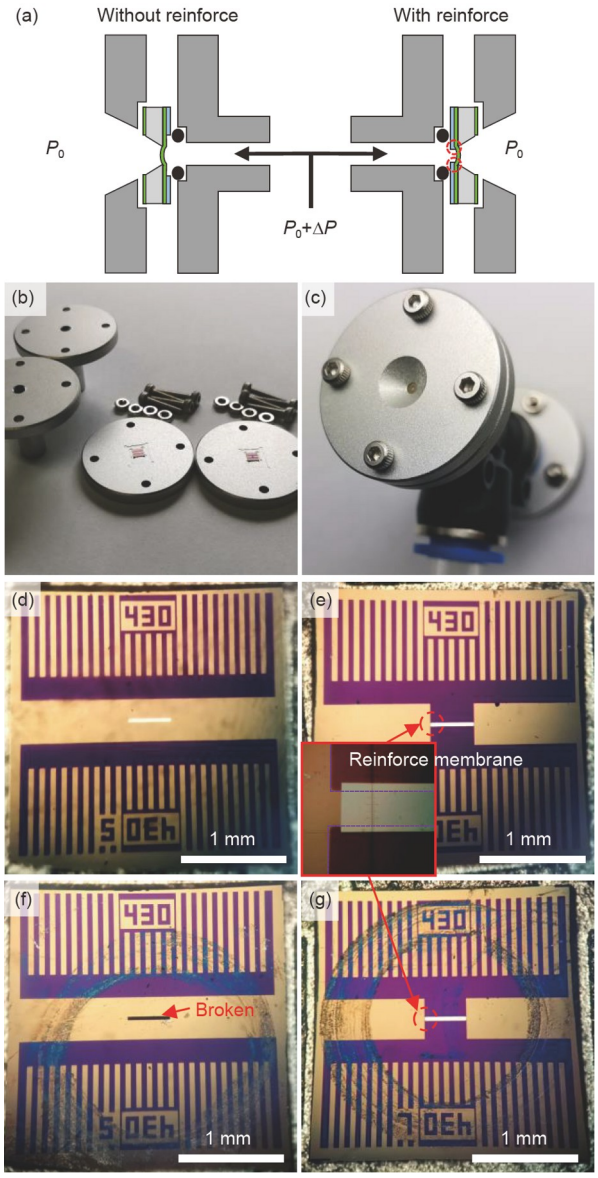


**Figure 5** The pressure endurance test for TEM chips with or without reinforcing structure. (a) The schematic of the pressure test. (b), (c) Optical images for the test setup. (d) The chip without reinforcing structure. (e) The chip with reinforcing structure. (f) The membrane broke after test and (g) membrane stays intact after air pressure differences with reinforcing structure.

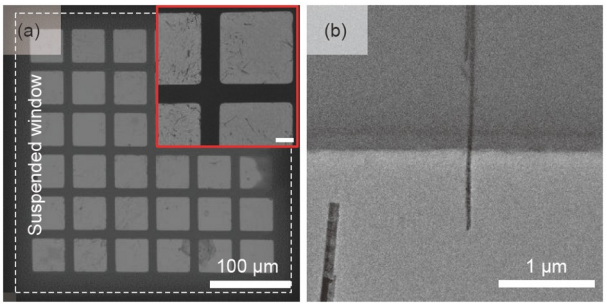


**Figure 6** TEM image of the large suspended window with stiffener structure (a). ZnO nanowires are loaded. Scale bar in the enlarged window is 10 μm. (b) Enlarged view on single ZnO nanowire.

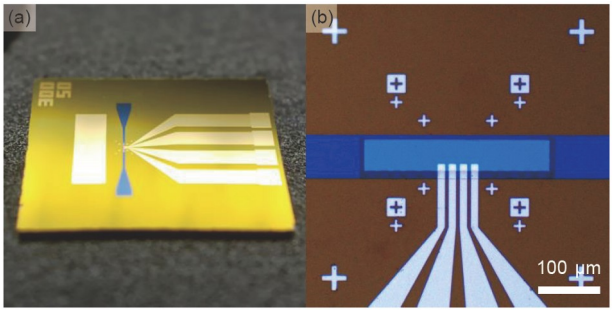


**Figure 7** (a) The chip view; (b) chip membrane window area. The marks and metal leads and reinforcing structure can be seen.

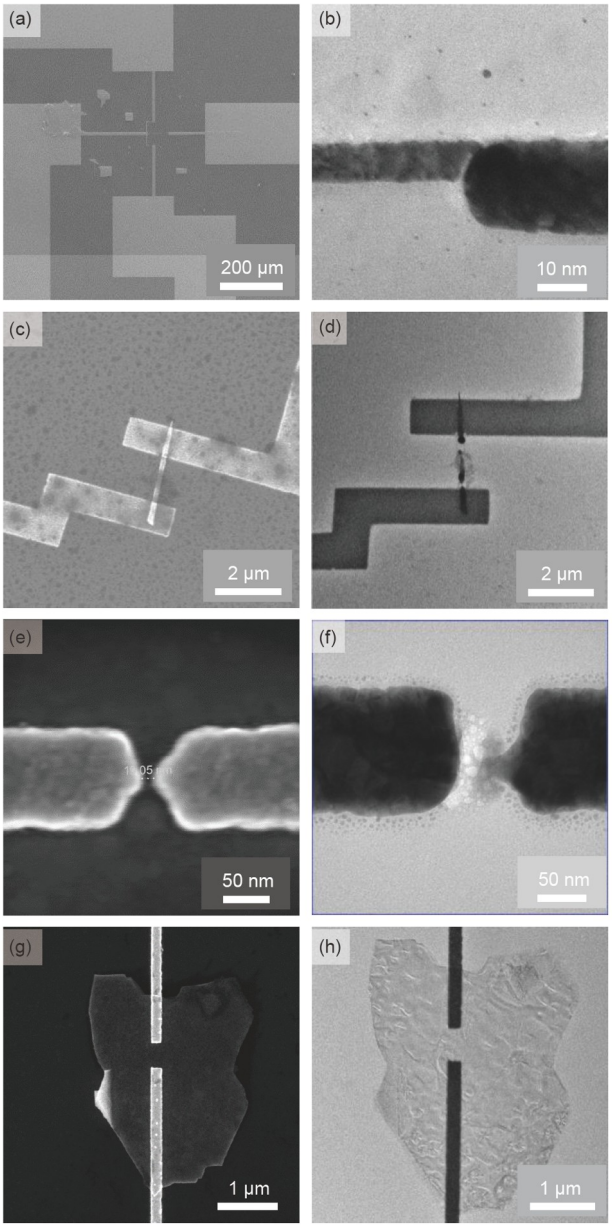


**Figure 8** The nanodevices fabricated using a semi-custom chip method. (a) The SEM and (b) TEM image of the metal nanogap-on-graphene device. (c) The SEM and (d) TEM image of InAs nanowire device. (e) The SEM and (f) TEM image of lateral resistive memory devices. (g) The SEM and (h) TEM image of a single $MoS_2$ device.

Figure 8(c) and (d) show an InAs nanowire device, which is prepared by contact transfer from the original substrate, then EBL and metal deposition. The high damage probability to the released membrane by smear transfer is avoided using our method implementation, resulting in a high yield.

Figure 8(e) and (f) show a transversal resistive memory with the nano-gap formation on a thin film of $TaO_x$ material. Our preparation method can be useful to study oxygen vacancy on the material surface while avoiding possible chemical damage to the nano-gap interface after device formation.

Figure 8(g) and (h) show $MoS_2$ devices. The 2D $MoS_2$ material is generated by tape tearing from bulk material and pressed directly onto the window area of the membrane unreleased chip, reducing the material transfer step and thus having the most lossless material properties.

Some nanomaterial research are also performed in our previous work using this methodology. The surface morphology evolution of ZnO during wet etching is studied by *in situ* liquid cell transmission electron microscopy [28].

Two-dimensional materials such as $MoS_2$ are generally transferred by solid pressing or liquid surface lifting. The transferred material is randomly distributed with a different number of layers and sizes. The larger the window, the higher the probability of finding the ideal material. After making optical and other observations, the location of the desired material can be located and fabricated into nanodevices with the customized post-fabrication process.

$MoS_2$ devices are sensitive to electron beam irradiation, this property allows $MoS_2$ devices to be used for radiology sensors. A $MoS_2$ device shown in Figure 8(h) is irradiated by the electron beam in TEM, and the irradiation effects are characterized.

In Figure 9(a), the SAED image and the diffraction spots of some crystalline surfaces marked therein show that this $MoS_2$ material in the device is a multilayered two-dimensional crystal. It can be seen that, at the first irradiation in Figure 9(b), the device conductivity increases substantially. The irradiation dose is $1.87\times10^{-5}$ $e^-/(Å^2\ s)$. The second irradiation is stronger, which dose is 1.15 $e^-/(Å^2\ s)$. It not only results in a faster current increase but also a later current decrease.

In the subsequent irradiation, the phenomenon that the current is larger after irradiation stopped than before irradiation could not be observed again. The main phenomenon is a linear like current drop during the 3rd irradiation, which is an 80 s 1.15 $e^-/(Å^2\ s)$, as shown in Figure 9(c). The current rises only during the irradiated period and returns to the same value as before irradiation when the irradiation stops, as the 6th to 10th weak irradiation shown in Figure 9(d).

Besides, the decreasing segment is clearly related to the irradiation intensity. To analyze the irradiation-induced current decreasing rate, the normalized slope is obtained by linear fitting and then dividing $I_{ON}$. Although the data points in Figure 9(e) are somewhat scattered, the slope ratio is related to the irradiation dose.

To analyze whether the saturation of the current rise caused by radiation is due to the sample being in a vacuum, we removed the sample from the electron microscope and inserted it again. A large increase similar to the first irradiation

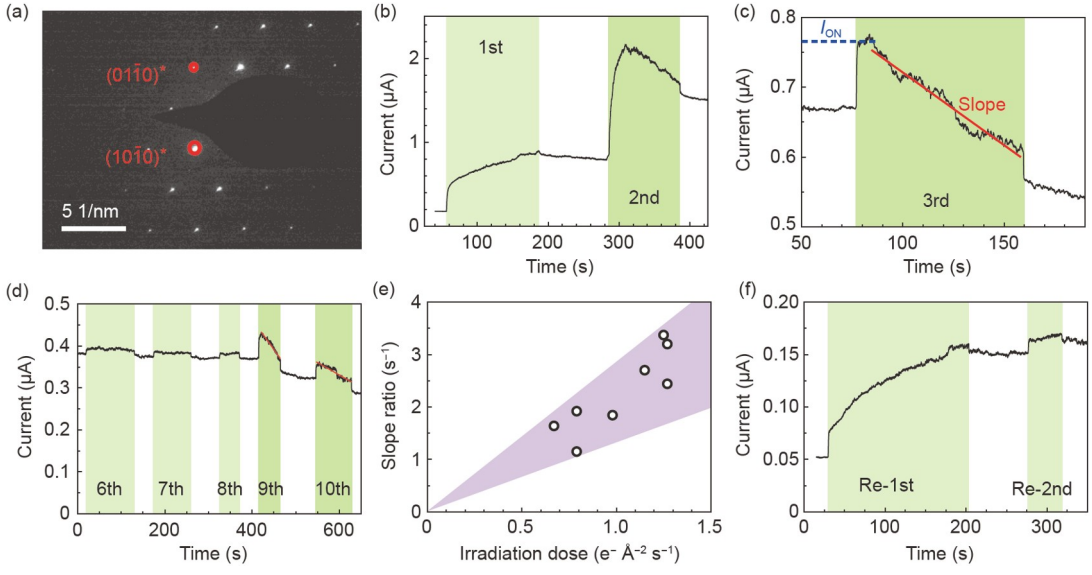


**Figure 9** (a) The selected area electron diffraction of the $MoS_2$ material. (b) The first and second electron beam irradiation responses in form of current versus time under 0.1 V applied voltage. The dose of electron beam irradiation applied during the time in the dark green pattern area is relatively large, and the dose of irradiation during the time in the light green pattern area is relatively small. (c) The electron beam irradiation induced current reducing response using the 3rd irradiation response as a sample. $I_{ON}$ is calculated at the beginning of the irradiation. The slope is linear fitted. (d) Multiple electron beam irradiation response from 6th to 10th. The voltage applied is 0.05 V. The dose of irradiations are $1.87\times10^{-5}$, $1.87\times10^{-5}$, $3.1\times10^{-7}$, 1.25 and 0.67 $e^-/(Å^2\ s)$. (e) The calculated slope ratio versus irradiation dose. (f) The irradiation response after the sample was taken out of TEM chamber and reloaded.

response is shown.

After irradiation, no discernible polycrystalline diffraction rings are seen in the diffractograms, and no diffraction spots are missing or added. This indicates that the irradiation damage did not significantly amorphized or change the crystalline state of $MoS_2$ crystals, and we can guess that the irradiation damage mainly points defect type of atomic deletion or bond breakage.

These electrical results demonstrate that the $MoS_2$ devices are well prepared and have good electrical signaling on the TEM chip.

The $MoS_2$ material used in the experiment is an n-type semiconductor that appears to turn on under positive gate control. Electron beam irradiation takes away electrons from the atoms of the material, resulting in the accumulation of positive charges in the material [45]. The charge in the electrically connected $MoS_2$ is only generated when irradiated, while the charge is stored in the isolated materials, such as the $SiN_x$ membrane suspending in the vacuum. So, there will be a current rise caused by charge accumulation, which can be seen only in the first few irradiations, after which it reaches saturation. This accumulation type current rise can be seen again after the device is released back into the air and reloaded. There is also a temporary charge increase in the device, which is reflected in the current rise during irradiation and the recovery after irradiation. In addition to accumulation mode and temporary charge increase, there is another factor that affects the device current. The electron beam is damaging the device material. It is irradiation dose-dependent and decreases the device current irreversibly.

## 4 Conclusion

In this paper, a methodology for *in situ* TEM observation and characterization of nanodevices and nanomaterials is proposed. Instead of riskily fabricating on the suspended membrane, the nanodevices and nanomaterials desired for study are securely added on a semi-customized TEM chip with an unreleased membrane window. Then, a membrane release technique is implemented to selectively and uniformly etch the silicon with a timely stop using the etching apparatus. The membrane reinforcement approach is later analyzed and validated, allowing larger window sizes to be applied. Next, TEM observation and *in-situ* electrical studies are performed on multiple devices, demonstrating the advantage of our methodology. Particularly, an electron beam-sensitive $MoS_2$ device is prepared and analyzed *in situ*. Overall, this study yields results that are instructive for device physics, demonstrating the reliability of the processing method we proposed.

*This work was supported by the National Key Research and Development Program of China (Grant No. 2016YFA0200802), and the National Natural Science Fundation of China (Grant No. 11890672).*

1 Creemer J F, Helveg S, Hoveling G H, et al. Atomic-scale electron microscopy at ambient pressure. Ultramicroscopy, 2008, 108: 993–998
2 Espinosa H D, Bernal R A, Filleter T. *In situ* TEM electromechanical testing of nanowires and nanotubes. Small, 2012, 8: 3233–3252
3 Ramachandramoorthy R, Bernal R, Espinosa H D. Pushing the envelope of *in situ* transmission electron microscopy. ACS Nano, 2015, 9: 4675–4685
4 Taheri M L, Stach E A, Arslan I, et al. Current status and future directions for *in situ* transmission electron microscopy. Ultramicroscopy, 2016, 170: 86–95
5 Wu J, Shan H, Chen W, et al. *In situ* environmental TEM in imaging gas and liquid phase chemical reactions for materials research. Adv Mater, 2016, 28: 9686–9712
6 Dai S, Gao W, Zhang S, et al. Transmission electron microscopy with atomic resolution under atmospheric pressures. MRS Commun, 2017, 7: 798–812
7 Jiang Y, Zhang Z, Yuan W, et al. Recent advances in gas-involved *in situ* studies via transmission electron microscopy. Nano Res, 2017, 11: 42–67
8 He B, Zhang Y, Liu X, et al. *In-situ* transmission electron microscope techniques for heterogeneous catalysis. ChemCatChem, 2020, 12: 1853–1872
9 Zhang C, Firestein K L, Fernando J F S, et al. Recent progress of *in situ* transmission electron microscopy for energy materials. Adv Mater, 2020, 32: 1904094
10 Zhang Y Z, Bu Y Q, Fang X Y, et al. A compact design of four-degree-of-freedom transmission electron microscope holder for quasi-four-dimensional characterization. Sci China Tech Sci, 2020, 63: 1272–1279
11 Creemer J F, Helveg S, Kooyman P J, et al. A MEMS reactor for atomic-scale microscopy of nanomaterials under industrially relevant conditions. J Microelectromech Syst, 2010, 19: 254–264
12 Ross F M. Opportunities and challenges in liquid cell electron microscopy. Science, 2015, 350: 1490
13 Wu F, Yao N. Advances in windowed gas cells for *in-situ* TEM studies. Nano Energy, 2015, 13: 735–756
14 Liao H G, Zheng H. Liquid cell transmission electron microscopy. Annu Rev Phys Chem, 2016, 67: 719–747
15 Kim B H, Yang J, Lee D, et al. Liquid-phase transmission electron microscopy for studying colloidal inorganic nanoparticles. Adv Mater, 2018, 30: 1703316
16 Pu S, Gong C, Robertson A W. Liquid cell transmission electron microscopy and its applications. R Soc Open Sci, 2020, 7: 191204
17 Spies M, Sadre Momtaz Z, Lähnemann J, et al. Correlated and *in-situ* electrical transmission electron microscopy studies and related membrane-chip fabrication. Nanotechnology, 2020, 31: 472001
18 Ye F, Xu M, Dai S, et al. *In situ* TEM studies of catalysts using windowed gas cells. Catalysts, 2020, 10: 779
19 Hultman L, Robertsson A, Hentzell H T G, et al. Crystallization of amorphous silicon during thin-film gold reaction. J Appl Phys, 1987, 62: 3647–3655
20 Jang M H, Agarwal R, Nukala P, et al. Observing oxygen vacancy driven electroforming in Pt-$TiO_2$-Pt device via strong metal support interaction. Nano Lett, 2016, 16: 2139–2144
21 Meister S, Schoen D T, Topinka M A, et al. Void formation induced electrical switching in phase-change nanowires. Nano Lett, 2008, 8: 4562–4567
22 Kumar P, Horwath J P, Foucher A C, et al. Direct visualization of out-of-equilibrium structural transformations in atomically thin chalcogenides. npj 2D Mater Appl, 2020, 4: 16
23 Inani H, Shin D H, Madsen J, et al. Step-by-step atomic insights into

structural reordering from 2D to 3D $MoS_2$. Adv Funct Mater, 2021, 31: 2008395
24 Almeida T P, McGrouther D, Pivak Y, et al. Preparation of high-quality planar FeRh thin films for *in situ* TEM investigations. J Phys-Conf Ser, 2017, 903: 012022
25 Gong Y, Zhang J, Jiang L, et al. *In situ* atomic-scale observation of electrochemical delithiation induced structure evolution of $LiCoO_2$ cathode in a working all-solid-state battery. J Am Chem Soc, 2017, 139: 4274–4277
26 Vijayan S, Jinschek J R, Kujawa S, et al. Focused ion beam preparation of specimens for micro-electro-mechanical system-based transmission electron microscopy heating experiments. Microsc Microanal, 2017, 23: 708–716
27 Sun M, Li X, Tang Z, et al. Constant-rate dissolution of InAs nanowires in radiolytic water observed by *in situ* liquid cell TEM. Nanoscale, 2018, 10: 19733–19741
28 Gorji S, Kashiwar A, Mantha L S, et al. Nanowire facilitated transfer of sensitive TEM samples in a FIB. Ultramicroscopy, 2020, 219: 113075
29 Textor M, de Jonge N. Strategies for preparing graphene liquid cells for transmission electron microscopy. Nano Lett, 2018, 18: 3313–3321
30 Boston R, Schnepp Z, Nemoto Y, et al. *In situ* TEM observation of a microcrucible mechanism of nanowire growth. Science, 2014, 344: 623–626
31 Tanta R, Kanne T, Amaduzzi F, et al. Morphology and composition of oxidized InAs nanowires studied by combined Raman spectroscopy and transmission electron microscopy. Nanotechnology, 2016, 27: 305704
32 Song B, He K, Yuan Y, et al. *In situ* study of nucleation and growth dynamics of Au nanoparticles on $MoS_2$ nanoflakes. Nanoscale, 2018, 10: 15809–15818
33 Huang X, Farra R, Schlögl R, et al. Growth and termination dynamics of multiwalled carbon nanotubes at near ambient pressure: An *in situ* transmission electron microscopy study. Nano Lett, 2019, 19: 5380–5387
34 Munch U, Brand O, Paul O, et al. Metal film protection of CMOS wafers against KOH. In: Proceedings of the International Conference on Micro Electro Mechanical Systems (MEMS). Miyazaki, 2000. 608–613
35 Canavese G, Marasso S L, Quaglio M, et al. Polymeric mask protection for alternative KOH silicon wet etching. J Micromech Microeng, 2007, 17: 1387–1393
36 Marsi N, Majlis B Y, Mohd-Yasin F, et al. ProTEK PSB as biotechnology photosensitive protection mask on 3C-SiC-on-Si in MEMS sensor. IOP Conf Ser-Mater Sci Eng, 2016, 160: 012093
37 Brugger J, Beljakovic G, Despont M, et al. Low-cost PDMS seal ring for single-side wet etching of MEMS structures. Sens Actuat A-Phys, 1998, 70: 191–194
38 Xu S Y, Xu J, Tian M L. A low cost platform for linking transport properties to the structure of nanomaterials. Nanotechnology, 2006, 17: 1470–1475
39 Wang Z, Yang F, Han D, et al. Alternative method to fabricate microdevices on a freestanding $Si_3N_4$ window. J Vacuum Sci Tech B Nanotechnol MicroElectron-Mater Proce Measure Phenomena, 2017, 35: 041601
40 Yu B, Li T, Yu P, et al. An interweaved-release silicon nitride film fabrication technique for mitochondrial vesicles electron microscopy. In: Proceedings of the International Conference on Miniaturized Systems for Chemistry and Life Sciences (MicroTAS). Savannah, 2017. 975–976
41 Tabata O, Tsuchiya T. Reliability of MEMS. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2008
42 Shafikov A, Schurink B, van de Kruijs R W E, et al. Strengthening ultrathin $Si_3N_4$ membranes by compressive surface stress. Sens Actuat A-Phys, 2021, 317: 112456
43 Pan R, Yang Y, Wang Y, et al. Nanocracking and metallization doubly defined large-scale 3D plasmonic sub-10 nm-gap arrays as extremely sensitive SERS substrates. Nanoscale, 2018, 10: 3171–3180
44 Yang Y, Pan R, Tian S, et al. Plasmonic hybrids of $MoS_2$ and 10-nm nanogap arrays for photoluminescence enhancement. Micromachines, 2020, 11: 1109
45 Li H, Liu C, Zhang Y, et al. Electron radiation effects on the structural and electrical properties of $MoS_2$ field effect transistors. Nanotechnology, 2019, 30: 485201