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Introduction of Interfacial Charges to Black Phosphorus for a Family of Planar Devices

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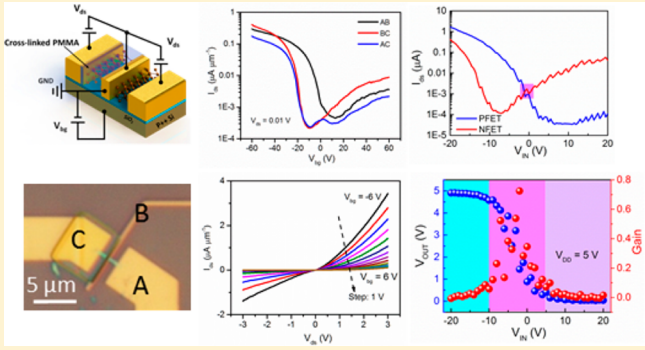
S *Supporting Information*

ABSTRACT: The capabilities to tune the conduction properties of materials by doping or electric fields are essential for the design of electronic devices. However, in two-dimensional materials substitutional doping has been achieved in only a few systems, such as Nb substitutional doping in MoS_2. Surface charge transfer is still one of the popular ways to control whether the conduction is dominated by holes or electrons. Here, we demonstrate that a capping layer of cross-linked poly(methyl methacrylate) modifies the potential in a black phosphorus (BP) layer so that conduction in the absence of an external electric field is dominated by electrons, rather than holes. Using this technique to form adjoining regions dominated by hole and electron conduction, a family of novel planar devices, such as BP-gated diodes, BP bidirectional rectifier, and BP logic inverters, can be fabricated. The devices are potentially useful for electronic applications, including rectification and switching.



KEYWORDS: *black phosphorus, interfacial charge, field-effect transistor, p−n diode, logic inverter*

The employment of two-dimensional (2D) layered materials as building blocks for next-generation nanoelectronics, represented by graphene[1] and transition metal dichalchogenides (TMDCs),[2] provides a possible alternative route for overcoming the scaling limits in Si-based complementary metal oxide semiconductor (CMOS) devices. The 2D nature of these layered materials confines the charge carriers to an atomically thin surface,[3,4] allowing transistors based on them to push the scaling limits and operation speeds beyond those of Si-based transistors.[5,6] Despite the extremely high mobility (~20 000 $cm^2/(V\ s)$) and the potential to approach ballistic transport at relatively large length scale (over hundreds of micometers),[7] lack of a finite band gap makes graphene unsuitable for logic applications that require a large current ON/OFF ratio ($>10^4$).[8] Semiconducting TMDCs, however, possess a finite and thickness-dependent band gap (ranging from ~0.5 to ~2.2 eV) but suffer from low carrier mobility.[2] The emergence of few-layered black phosphorus (BP) as the channel material for FETs fills the gap between graphene and TMDCs due to its moderate bandgap (0.3 eV for bulk and 2.0 eV for monolayer) and a high hole mobility of ~1000 $cm^2/(V\ s)$.[9−11] Because of the bandgap, a current ON/OFF ratio of 5 orders of magnitude has been realized in BP FETs.[9−11] However, due to the Schottky barrier formation between the metal contact electrodes and BP,[9,11−14] a strong asymmetry in electron and hole transport in BP FETs has been observed.[15−18] The hole mobility and the current on/off ratio in FETs based on hole conduction are several orders of magnitude higher than the electron mobility and the on/off ratio of FETs based on electron conduction, resulting in a great challenge in realization of complementary devices in a single BP flake. Until recently, electron doping and complementary device based on a single BP flake has been achieved.[19]

In conventional semiconductor devices, n-type or p-type behavior is obtained by substitutional doping. In 2D materials, however, due to their stable lattice structures and absence of dangling bonds, substitutional doping has been only achieved in a few systems, such as Nb substitutionally doped MoS_2.[20,21] The conductivity type (holes vs electrons) can be modified by electrostatic modulation via an external electrical field, but the

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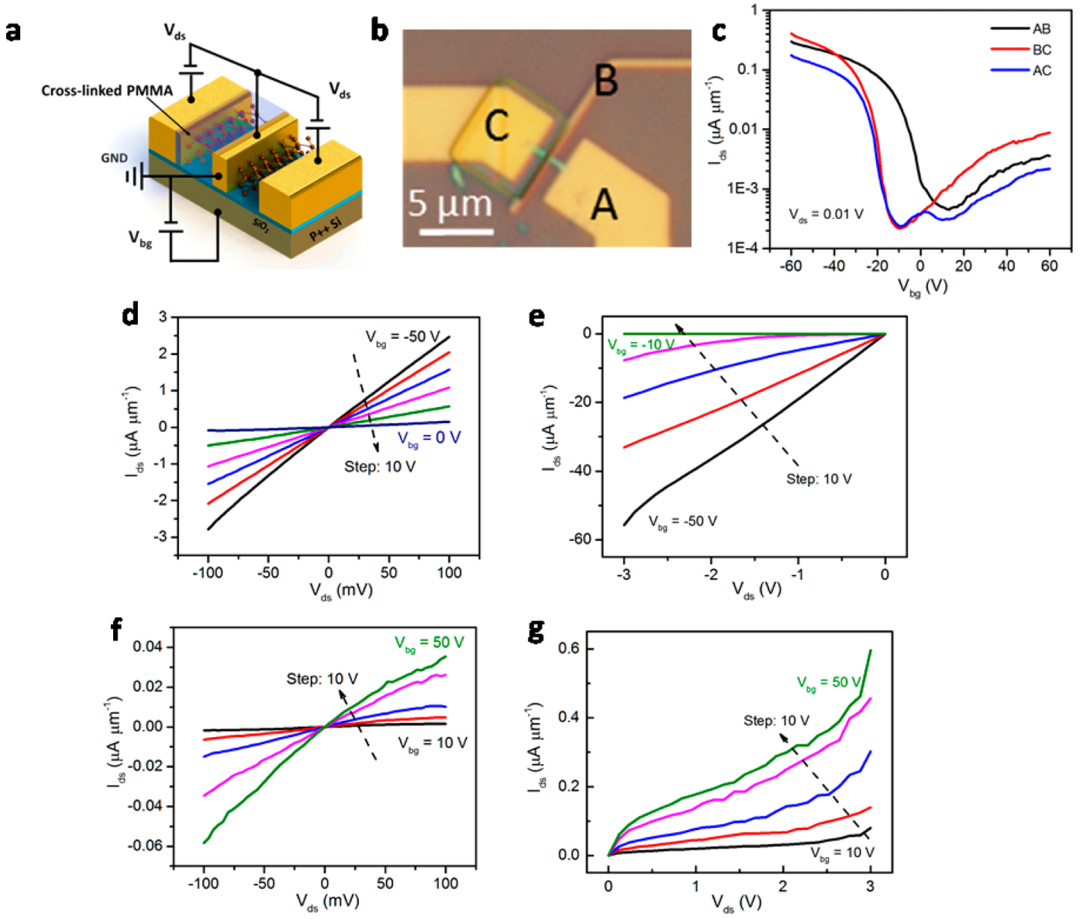

Figure 1. Electrical characterization of few-layer BP FETs with and without cross-linked PMMA as capping layer using Cr/Au (5/60 nm) metal stacks as contact electrodes. (a) Schematic of BP FET devices with and without cross-linked PMMA as capping layer in the same channel and their measurement setup. The brown balls and sticks stand for the BP lattice. (b) Optical image of the device. Cr/Au (5/60 nm) metal stacks are used as contract electrodes. (c) Source-drain current (logarithmic scale) of pure BP FET (black curve, AB), cross-linked PMMA-covered BP FET (red curve, BC), and BP p−n diode (blue curve, AC) as a function of gate voltage from a 10 nm-thick BP flake at room temperature with drain-source voltage of 100 mV. (d) *I*−*V* (output) characteristics of pure BP FET (AB) on the hole conduction side with negative gate bias ranging from −50 to 0 V in a step of 10 V. The observed linear behavior indicates a good contact. (e) Source-drain current of pure BP FET (AB) under large voltage bias (−3 to 0 V) with gate voltage modulation ranging from −50 to 0 V in a step of 10 V, indicating a typical P-FET behavior. (f) *I*−*V* (output) characteristics of cross-linked PMMA-capped BP FET (BC) on the electron conduction side with positive gate bias ranging from 10 to 50 V in a step of 10 V. The nonlinear behavior indicates the formation of a Schottky barrier at the contacts. (g) Source-drain current of cross-linked PMMA-capped BP FET (BC) under large voltage bias (−3 to 0 V) with gate voltage modulation ranging from −50 to 0 V in a step of 10 V, indicating a typical n-FET behavior, such as current saturation a punch-through state under large bias (around 3 V).

efficiency is rather limited because of the lack of good interfaces between high quality thin dielectrics and 2D materials. Another way of controlling the conductivity type is based on capping the 2D materials with a layer of polymer or absorbing specific gas molecules and adatoms,[19] or even dielectric engineering.[5] These capping layers avoid complicated device fabrication processes and produce negligible damage to the lattice structure of the underlying 2D materials. Previous work reported that capping BP layers with Al_2O_3 or MoO_3 results in ambipolar transport dominated by hole conduction in the absence of an external electric field,[13,18] where charge transfer between the capping layer and the BP determines the conductivity type.[17] Ambipolar transport dominated by electrons was observed in Cs_2CO_3-capped BP layers.[18] Recently, BP FETs with Al_2O_3 as the top gate dielectric on glass[22] and flexible polyimide substrates[23] have been reported using a dual gate configuration.

Poly(methyl methacrylate) (PMMA) is a typical positive photoresist used in electron beam lithography. Exposure with moderate-dose (typically 100−120 $\mu C/cm^2$) electron irradiation causes chain scissions, while high irradiation dose exposure (typically >15 000 $\mu C/cm^2$) produces cross-linking. The cross-linked PMMA may be used as a dielectric through which an external voltage can be used to modulate the conductivity of materials through the field effect.[24] However, the effect of oxygen-containing molecular groups (such as CH_3OOC^-) generated during the cross-linking process has not been reported.[25] Here, we demonstrate that capping a thin BP layer with a layer of cross-linked PMMA modifies the conductivity type of the BP by a surface charge transfer process, converting a BP layer dominated by hole conduction in the absence of an external electric field to one dominated by electron conduction. Combining BP films capped by cross-linked PMMA with standard BP, a family of planar devices can be created, including BP-gated diodes (standard BP layer and cross-linked PMMA-capped BP layer in series, sharing a common back gate), and BP bidirectional rectifier (concatenating two back-to-back BP gated diodes in series in which a gate-tunable potential barrier is established between the cross-linked

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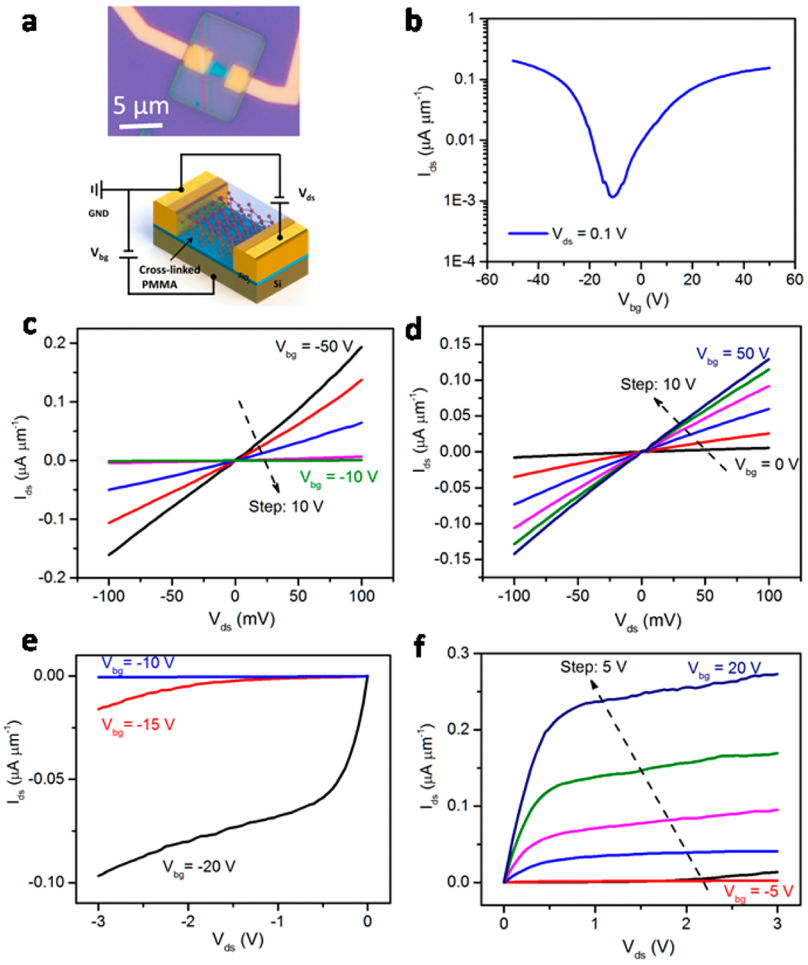

Figure 2. Electrical characterization of cross-linked PMMA-capped BP FET with Ni/Au (5/60 nm) metal stacks as contact electrodes. (a) Optical image (upper panel) and schematic (lower panel) of BP FET fully capped with cross-linked PMMA. (b) Source-drain current (logarithmic scale) of cross-linked PMMA-capped BP FET as a function of gate voltage with source-drain voltage of 0.1 V, showing the ambipolar transport behavior with the almost the same magnitude modulation for holes and electrons conduction. (c,e), $I-V$ characteristics of the device on the holes conduction side at varying bias range. The near-linear behavior in (c) suggests a good contact nature, whereas in (e) a current saturation behavior is clearly observed. (d,f), $I-V$ characteristics of the device on the electrons conduction side at varying bias range. The linear relationship between current and voltage in (d) indicates an effective reduction of the Schottky barrier at the contacts, whereas in (f) an apparent current saturation behavior is demonstrated.

PMMA-capped and uncapped regions). These devices are capable of performing either unidirectional current rectification (BP-gated diode, rectification ratio >10^2) or bidirectional current rectification (BP bidirectional rectifier, rectification ratio ~10^2), and signal inversion (BP logic inverter, gain ~0.75) operations. The device performance demonstrated here suggests a promising route for developing 2D-based electronics.

BP FETs with and without Cross-Linked PMMA as Capping Layer. BP flakes with thickness of 8−10 nm are mechanically exfoliated in a glovebox onto p++ doped Si substrates with 300 nm thermal oxidized SiO_2 serving as the back gate dielectric. To protect the BP flakes from ambient degradation before they are exposed to atmosphere, a layer of PMMA (495, 2% in anisole) is spin coated. For contact electrode definition and a better lift-off process, an additional layer of PMMA (950, 5% in anisole) is spin coated. (Details can be found in Supporting Information Figure S1.) All electrical characterization is performed in a vacuum chamber with a vacuum level of ~10^{-6} Torr. To investigate the effects of cross-linked PMMA capping layers on the transport properties of the underlying BP, part of the BP flake is covered, as schematically shown in Figure 1a. Figure 1b shows a typical optical image of the device with Cr/Au (5/60 nm) contact electrodes, in which electrodes A and B coupled with a pure BP region (not capped by cross-linked PMMA) compose a pure BP FET, while electrodes B and C coupled with a cross-linked PMMA-capped BP region compose a cross-linked PMMA-capped BP FET. Figure 1c shows the transfer characteristics of a pure BP FET (black curve) and a cross-linked PMMA-capped BP FET (red curve). The pure BP FET shows ambipolar transport[26] dominated by hole conduction at zero gate voltage with current modulation of ~10^3, which is consistent with previous reports.[9−13,18,27−31] For V_{bg} < 0, the output characteristics of the pure BP FET with small (Figure 1d) and large (Figure 1e) source-drain bias, show a well-defined p-channel FET behavior. For V_{bg} > 0, corresponding to electron conduction (Figure 1f,g), the output characteristics of cross-linked PMMA-capped BP FET show a strong nonlinear behavior (Supporting Information Figure S3), indicating a Schottky contact.[9] Compared with the pure BP FET, the transfer characteristics of the cross-linked PMMA-capped BP FET show ambipolar behavior, dominated by electron conduction at zero gate voltage and characterized by a negative threshold voltage (red curve in Figure 1c), suggesting positive charges are introduced

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at the interface between the cross-linked PMMA and the BP surface, resulting in electrons in the BP layer as previously reported using Al_2O_3 and Cs_2CO_3 as the capping layer.[13,17,18,32] The amount of interfacial charge can be controlled by varying the electron beam dose used to irradiate the PMMA, characterized by the successive shift of the current−voltage characteristics to more negative voltages with increasing dose (Supporting Information Figure S8). Furthermore, capping with cross-linked PMMA yields enhanced electron transport behavior, including improved magnitude of current modulation on the electron conduction side of the transfer characteristics (red curve in Figure 1c) and a near-linear relationship in the output characteristics (Figure 1f,g), indicating an effective reduction of Schottky barrier height at the contact edge.[17,18] As for the carrier mobility, in the pure BP FET hole and electron mobilities are extracted from the transfer curve in Figure 1c as 90.7 and 1.4 $cm^2/(V\ s)$, respectively, whereas in the cross-linked PMMA-capped BP FET, they are 175.4 and 3.0 $cm^2/(V\ s)$ (Supporting Information Figure S6), respectively. The enhanced carrier mobility can be attributed to the improvement of contact features.[18]

Considering that Ni has higher work function (5.0 eV) than Cr (4.5 eV), it is expected that using Ni as contact electrodes will provide a better contact to regions dominated by hole conduction, based on ideal metal−semiconductor contact theory.[8] To further investigate the effect of the cross-linked PMMA-capping layer on the transport properties, we fabricated a BP FET fully capped with cross-linked PMMA using Ni/Au (5/60 nm) as the contact electrodes, as schematically shown in the lower panel of Figure 2a. The upper panel of Figure 2a shows an optical image of the device. Surprisingly, the transfer characteristic of the device shown in Figure 2b indicate that using Ni/Au stacks as contact electrodes favors electron transport, resulting in more symmetric ambipolar transport with almost the same current modulation for holes and electrons, $\sim 10^2-10^3$, indicating a more symmetric band alignment compared to that of Cr (Figure 1c). Previous reports suggested that for thin (<3 layer) BP flakes, metal contacts with both large (Pd, 5.2 eV) and small (Ti, 4.35 eV) work function can favor hole conduction, indicating Fermi level pinning is present at the contact interface.[13] For thick (>20 layers) BP flakes, metal contacts with lower work function (Ni, 5.0 eV) result in better ambipolar transport compared to that of higher work function metal (Pd, 5.2 eV), suggesting no Fermi level pinning at the contacts.[12] In our case, larger work function Ni contacts lead to better ampipolar transport compared to that of Cr contacts (Figure 1c), indicating a lower Schottky barrier height and better carrier injection efficiency from the Ni contact. This can be further verified by the output characteristics of the device, as shown in panels c−f in Figure 2. Under small source-drain bias (from −100 to 100 mV), both for electron ($V_{bg} > 0$, Figure 2d) and hole conduction ($V_{bg} < 0$, Figure 2c), the current shows a strong linear relationship, indicating a smaller Schottky barrier height compared to that of Cr (Supporting Information Figure S4). Under large source-drain bias, for the parts of the current−voltage relationship dominated by holes (Figure 2e) and electrons (Figure 2f), the device shows pronounced current saturation, suggesting the successful realization of both BP p-type FETs (PFET) and n-type FETs (NFET). The availability of BP PFETs and NFETs inspires us to construct BP complementary circuits.

BP-Gated Diodes. On the basis of the electron-dominated conductivity of cross-linked PMMA-capped BP regions and the hole-dominated conductivity of pure BP regions, we can construct a BP diode by combining a pure BP FET and cross-linked PMMA-capped BP FET in series, as schematically shown in Figure 1a. Note that this is not a conventional PN diode because of the metal contact separating the two regions, although it does exhibit some analogous behavior. Figure 3a shows the linear plot of output characteristics of a representative device under different gate bias (ranging from −5 to 5 V in a step of 2 V). A logarithmic plot is shown in Figure 3b. From the output characteristics, we can see that at V_{bg} = −5 and −3 V, there is little rectification because both regions are dominated by hole conduction at this gate bias. For the other gate voltages, the device shows good rectification behavior with gate tunable rectification ratios (Supporting Information Figure S7). The rectification is produced by the asymmetry in the hole and electron conduction branches, shown in Figure 1c. Because of the middle contact, the current−voltage relationship is not described by a Boltzmann relationship (either the ideality factor is far larger than 2 or the fit is poor (r^2 < 70%)), as shown in Supporting Information Figure S7. The transfer curve (blue curve in Figure 1c) further demonstrates the gate tuning capability of the BP diode. The current on/off ratio is in the range of 10^3-10^4, satisfying the requirements of logic operations. The two valleys (conduction minima) in the transfer curve (blue curve in Figure 1c) correspond to the depleted states of the cross-linked PMMA-capped BP and pure BP, respectively. As previously reported for

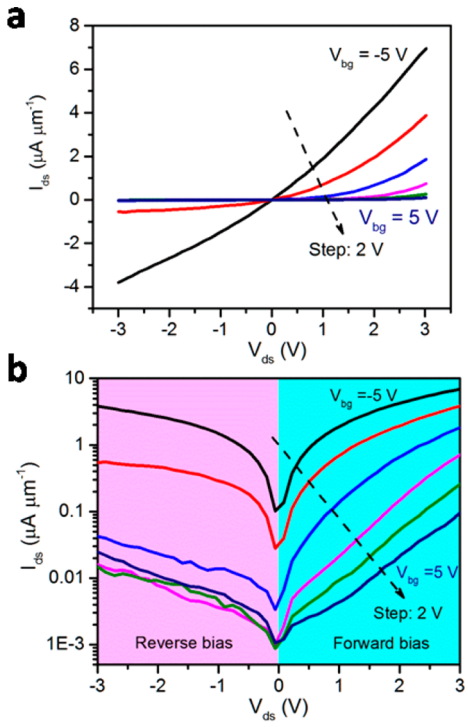

Figure 3. Electrical characterization of BP p−n diodes with Cr/Au (5/60 nm) metal stacks as contact electrodes. (a) Linear plot of *I*−*V* (output) characteristics of BP diode (shown in Figure 1b) under gate voltage modulation ranging from −5 to 5 V in a step of 2 V. The typical rectification behavior reveals the formation of BP diode, and reverse bias punch-through under large gate voltage (−5 V, black curve). (b) Logarithmic plot of the current output characteristics, suggesting a gate-tunable rectification behavior with a highest rectification ratio of ∼100 under large back gate voltage (3 V).

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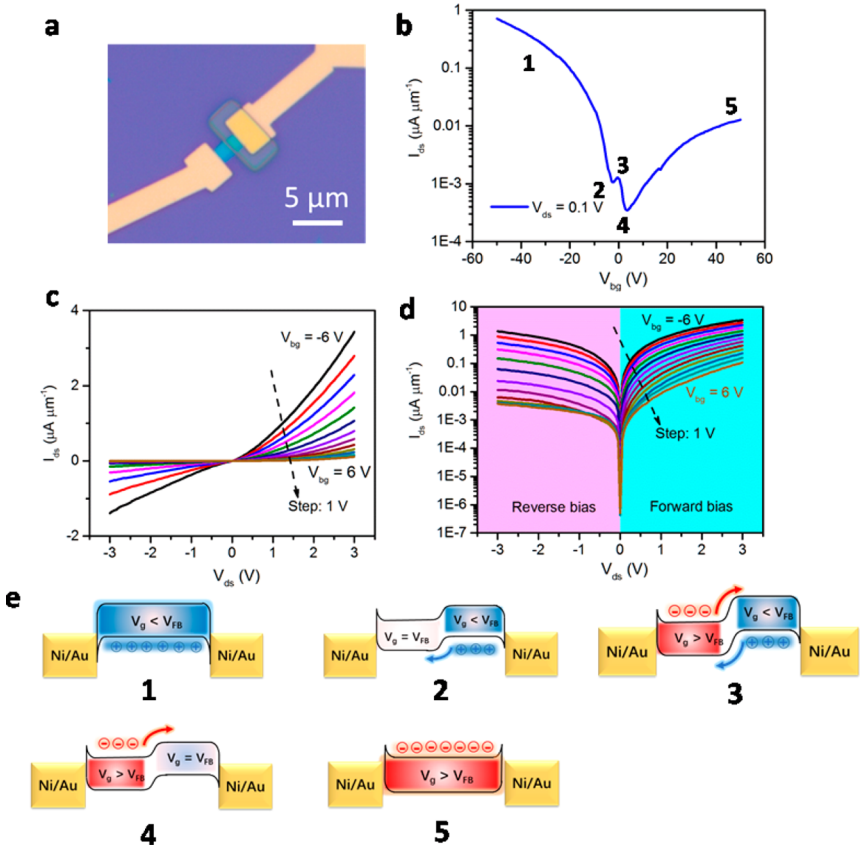

Figure 4. Electrical characterization of BP p−n diodes with Ni/Au (5/60 nm) metal stacks as contact electrodes. (a) Optical image of BP p−n diode fabricated by partially capped the BP conduction with cross-linked PMMA. Contact electrodes are made of Ni/Au (5/60 nm) stacks. (b) The forward diode current as a function of back gate voltages at constant source-drain bias of 0.1 V. (c) Current versus bias voltage under gate voltage modulation in the range of −6 to 6 V with a step of 1 V. (d) Logarithmic plot of the current−voltage characteristics in (c). Bipolar switching behavior of the device can be observed in both reverse (pink background) and forward bias (blue background) regimes, showing both reverse bias and forward bias have a high current on/off ratio (close to 10^5 at forward bias and gate voltage of 6 V). The lowest current can reach 10^{-6} μA μm^{-1}, showing a completely "off" state. (e) Schematic diagram of the energy band at the points labeled as "1", "2", "3", "4", and "5" in transfer curve of the device shown in (b)."1" and "5" represent the holes conduction and electron conductions, respectively. "2"and "4" stand for flat-band for holes and electrons conduction, respectively, and "3" stands for the potential barrier that is built-up between the capped region and uncapped region.

a carbon nanotube-MoS_2 heterojunction p−n diode,[33] the transfer curve of the BP diode can be qualitatively viewed as a superposition of the transfer curves of the p-type pure BP FET (black curve in Figure 1c) and the n-type cross-linked PMMA-capped BP FET (blue curve in Figure 1c), except that the net current flowing through the diode is smaller than that of pure BP FET and capped BP FET on the electron conduction side. As discussed above, Ni has a better band alignment than Cr when in contact with BP (Figure 2).

To examine contact effects, we fabricated BP diodes using Ni/Au (5/60 nm) as the contact electrode and to avoid the formation of an additional Schottky barrier the middle electrode was removed. A representative optical image of such a device is shown in Figure 4a. Figure 4c shows the output characteristics of the device under gate bias modulation ranging from −6 to 6 V with a step of 1 V and Figure 4d is a logarithmic plot. Current rectification behavior also is observed for this device. Compared to devices using Cr/Au as the contact metal, the reverse current shows a clear saturation behavior at large reverse bias, confirming the improvement of contact features. At gate biases ranging from −6 to −3 V, the device does not exhibit significant rectification, while at other gate biases, the device shows a typical diode behavior with a gate-tunable rectification ratio ranging from ∼2 to ∼70 (Supporting Information Figure S13). Although the rectification ratio is relatively low compared to other 2D material-based diodes,[27,33−39] our device shows a pronounced bipolar current switching behavior. Under reverse bias (light magenta shaded region in Figure 4d), the device shows an apparent current saturation behavior at large reverse bias voltages, and both the on-state current, I_{on}, and the off-state current, I_{off}, determined by the height of potential barrier can be modulated by V_{bg}, yielding an I_{on}/I_{off} ratio of $\sim 10^3-10^4$. Under forward bias (light cyan-shaded region in Figure 4d), the current does not saturate and shows switching operation with an I_{on}/I_{off} ratio of 10^4-10^5 at V_{ds} = 3 V (Supporting Information Figure S13). Figure 4b shows the current modulation of the diode for V_{bg} ranging from −60 to 60 V at a forward bias of 0.1 V. Under gate bias modulation, the diode transitions from a p−p junction at V_{bg} = −50 V (labeled as "1") to an n−n junction at V_{bg} = 50 V (labeled as "5"), during which two valleys appearing at V_{bg} = −2 and 3.5 V (labeled as "2" and "4", respectively) reveal the depletion state for the capped BP (p−i junction) and pure BP (n−i junction), respectively. The peak at V_{bg} = −0.4 V (labeled as "3") indicates the formation of a potential barrier between the capped and uncapped regions. Band diagrams of these featured points are schematically shown in Figure 4e, indicating the progressive tuning of the potential barrier.

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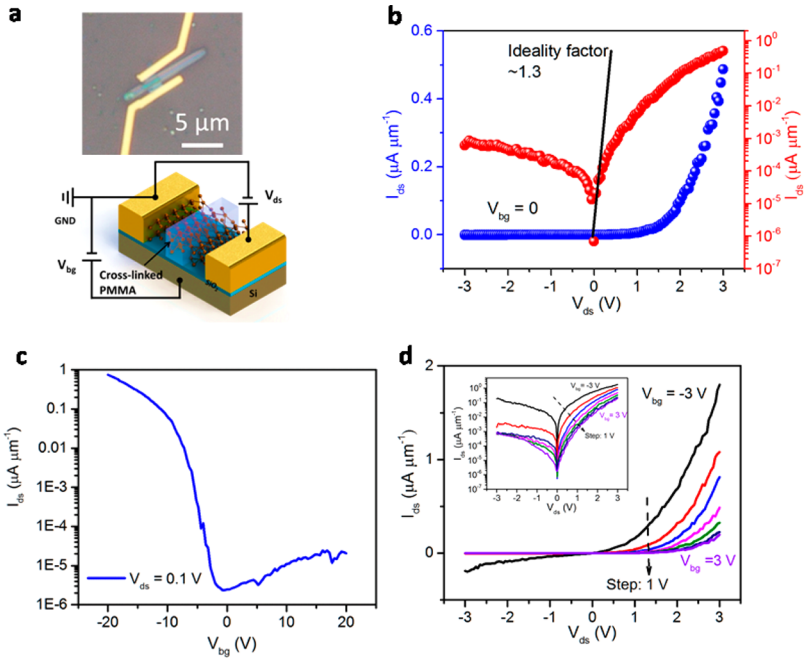

Figure 5. Electrical characterization of BP bidirectional rectifier composed of two BP diodes in back-to back series. (a) Optical image (upper panel) and schematic diagram (lower panel) of the device composed of two identical BP diodes in back-to-back series. Ni/Au (5/60 nm) stacks are used as contact electrodes and for efficient gate modulation, SiO_2 layer of 100 nm is used as gate dielectric. (b) Source-drain current as a function of both reverse and forward bias voltages at V_{bg} = 0. Blue scatters show the linear plot, while red scatters show the logarithmic plot. Fitting the logarithmic plot at small bias with Schockley's equation yields an ideality factor of ~1.3. (c) Source-drain current as a function of gate voltage bias at a constant source-drain current of 0.1 V. (d) Source-drain current versus bias voltage under gate voltage modulation ranging from −3 V to +3 V in a step of 1 V. Inset is the logarithmic plot.

BP Bidirectional Rectifier. The combination of cross-linked PMMA-capped and pure BP FETs in series yields a back-gated BP diode. What if we combine two gated BP diodes back-to-back in series? This configuration is schematically shown in the lower panel of Figure 5a and the upper panel is an optical image of a representative device. We can realize it by placing a strip of cross-linked PMMA at the central part of a normal pure BP FET. Figure 5b shows the current as a function of bias voltage for the device at V_{bg} = 0. At reverse bias and low forward bias, the current is on the order of 10^{-11}−10^{-9} A, corresponding to the off state. When the forward bias reaches 1 V, the current shows a rapid, near-exponential, increase. Moreover, as the bias increases from 0 to 0.05 V, the current increases by almost 2 orders of magnitude, a hallmark of diode behavior. Fitting the data in the low bias voltage range with Schockley's equation yields an ideality factor of ~1.3. The rectification ratio is ~10^2. Because of the symmetric configuration of the device (Figure 5a), the capability of rectification should not depend on the voltage bias direction. As shown in Supporting Information Figure S15, when the bias direction is changed, the device shows almost the same rectification behavior. In this regard, this device is called BP bidirectional rectifier. If the strip of cross-linked PMMA was placed off the central part of the transport channel, an asymmetric BP bidirectional rectifier is obtained. The schematic and scanning electron microscopy (SEM) image of the device is shown in Supporting Information Figure S16a. The output characteristics of the device shown in Supporting Information Figure S16c,d clearly shows its asymmetric rectification behavior. If the contact region of the device is capped by two strips of cross-linked PMMA, respectively, similar bidirectional rectification behavior can be observed, as shown in Supporting Information Figure S17. The capped region shows electron-dominated conduction (Figure 1d), while the bare BP at both sides shows hole-dominated conduction. Because introduction of charges by the cross-linked PMMA-capping layer at the interface creates an electrostatic potential that can be considered as an "effective top gate" and shifts the Fermi level of the BP under the capped region, a gate-tunable potential barrier[24] can be built up between the cross-linked PMMA-capped region and the uncapped region. When the device is biased, both majority holes and minority electrons will cross the potential barrier through diffusion once they gain enough energy (V_{bg} = 0, V_{ds} > 0, Figure 5b).[24] The capping layer of cross-linked PMMA, serving as an "effective" top gate, tunes the Fermi level of the capped region, while the global back gate voltage can tune the carrier density in the whole BP transport channel. Correspondingly, the height of the potential barrier can be tuned through V_{bg} modulation. To enhance the back gate modulation efficiency, a 100 nm SiO_2 layer is used as the gate dielectric and to reduce the contact resistance, Ni/Au (5/60 nm) is used as the contact metal. Figure 5d shows the typical output characteristics of the BP bidirectional rectifier under V_{bg} modulation from −3 to 3 V and the inset shows the same data in a logarithmic plot. The rectification behavior of the device is indicated by the steep increase of the current (I_{ds}) once the bias voltage (V_{ds}) surpasses the turn-on voltage V_{to}. The turn-on voltage is defined where the current exceeds the reverse-bias saturation current. V_{to} can be tuned between 0 and 0.85 V when sweeping V_{bg} from −3 to 3 V. A logarithmic plot of the output curve suggests that the BP bidirectional rectifier can work in two different regimes, as shown in the inset of Figure 5d. In the first regime, the BP bidirectional rectifier behaviors like a conventional FET when it is reverse-biased,

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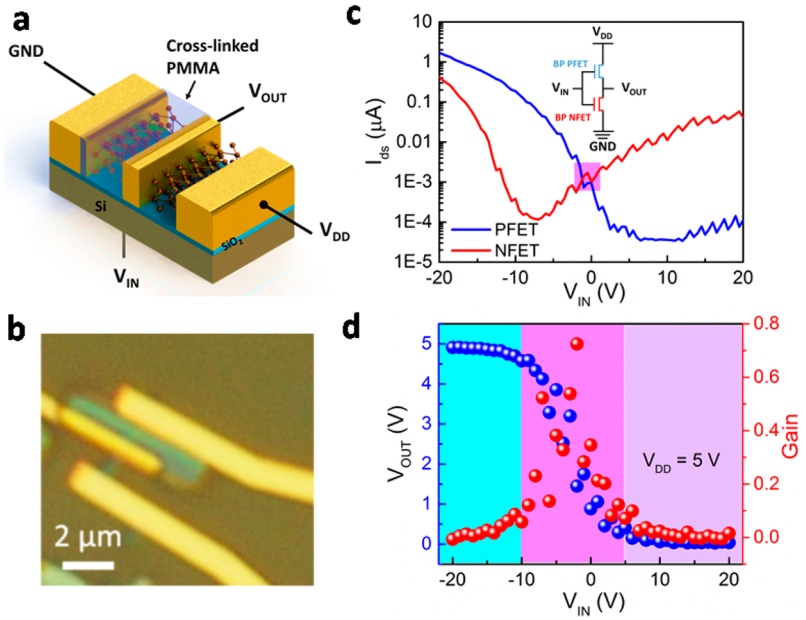

Figure 6. Electrical characterization of a few-layer BP logic inverter. (a) Schematic diagram of the logic inverter. (b) Optical image of the BP logic inverter. (c) Transfer characteristic of BP PFET and BP NFET realized by capping of cross-linked PMMA, showing their PFET and NFET behaviors, respectively. Inset is an equivalent circuit diagram. The enclosed pink window indicates the region where the inverter has the highest output gain. (d) The output voltage and gain as a function of input voltage, showing a highest gain of 0.75 is obtained. The cyan-, pink-, and violet-shaded areas indicate three different working regimes of the BP logic inverter.

where the current shows a tendency to saturate at large reverse-bias voltages. A current on/off ratio of 10^2–10^3 can be obtained, in which the off current is located at the greatest attainable potential barrier. In the second regime, the BP bidirectional rectifier works like a diode when it is forward-biased. The current increases exponentially at large bias voltages and does not saturate. Near the turn-on voltage, with V_{bg} modulation the current can be varied by several orders of magnitude, indicating switching operation with high current on/off ratio. The blue curve in Figure 5d shows the switching operation of the BP bidirectional rectifier when it is in a forward-biased state, revealing a high on/off ratio of 10^5–10^6. This suggests that our BP bidirectional rectifier has promising applications in digital switching devices and current rectifiers without considering the bias direction.

BP Logic Inverter. Finally we demonstrate a logic inverter based on a cross-linked PMMA-capped ambipolar BP FET and a BP ordinary FET. Figure 6a shows a 3D cartoon of the device fabricated on an individual BP flake by capping the half portion of the ordinary BP FET with cross-linked PMMA. The BP NFET function is realized in the capped region and the PFET function is realized in the uncapped region (Figure 1). V_{IN}, the input voltage, is applied to the back gate. V_{OUT} is the output voltage and V_{DD} is the supply voltage. Figure 6b is a photograph of the BP logic inverter based on our cross-linked PMMA-capped BP NFET and pure BP PFET. Figure 6c shows the transfer characteristics as a function of input voltage V_{IN}. The capping of cross-linked PMMA induces a threshold voltage (or charge neutrality point) shift, where the capping layer works like an effective top gate and shifts the Fermi level of the capped region. This results in NFET-like operation (indicated by the negative charge neutrality point in the transfer curve shown in Figure 6c). The input voltage V_{IN} can tune the carrier density of the whole BP transport channel and combine with the cross-linked PMMA "top gate" to generate the inverted signal, V_{OUT}. Figure 6d shows the output voltage and gain of the inverter as a function of input voltage. The output voltage shows three different regimes. In the first regime (cyan-shaded region), with the input voltage V_{IN} between −20 and −10 V, the output voltage is in the "high" state with a tendency to drop with a flat slope, and correspondingly, the gain (G), defined as the slop of the output characteristics,[13] that is $G = dV_{OUT}/dV_{IN}$, gently increases. When the input voltage V_{IN} is between −10 and 5 V (pink-shaded region), the output voltage V_{OUT} shows a transition from the "high" to "low" (V_{OUT} = ∼0) state with a steep slope and the gain follows a Dirac-δ function like behavior with a highest value of 0.75. An ideal logic inverter should have an infinite gain and no such transition in output voltage occurs. When the input voltage V_{IN} is further increased, the output voltage V_{OUT} stays steadily at the "low output" state with a near zero value. From the transfer curves of the BP NFET and PFET (shown in Figure 6c), we can see that the transition regime of the inverter covers the steepest portion of the subthreshold region of both the BP NFET and PFET; consequently, the highest gain appears in this region, indicated by the pink shaded region in Figure 6c. One limiting factor of the low gain of the inverter is that the subthreshold slopes of the BP PFET and NFET at the crossover region (indicated by the pink box in Figure 6c) are 2.5 and 5.3 V/decade, respectively, which is much greater than the ideal slope of 60 mV/decade. The other factor limiting the gain of the inverter is the current saturation behavior in the device. As shown in Supporting Information Figure S17b, the output characteristic of PFET does not show an expected saturation behavior, which inevitably reduces the gain of the inverter. From the output curve shown in Figure S17c, the BP NFET shows a Schottky contact behavior, indicating that contact resistance is also a limiting factor. Using a thinner gate dielectric, or a high-k dielectric, like HfO_2, and lower contact resistance will result in enhancement of the gain.[13] Another key parameter for logic inverter applications is

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the matching of output and input voltages. Compared to previous reports on logic inverters based on MoS_2,[27,40] WSe_2,[41] black phosphorus,[19,27] and so forth, our BP logic inverter shows a small mismatch of output and input voltages (Figure 6c). This mismatch probably comes from the shift of the transfer curve of PFET toward negative input voltages, which is induced by desorption of O_2 or H_2O at the exposed BP surface when the current passes through the channel. Capping the exposed BP part with a stable and undoped layer, such as BN, will prevent the adsorption of O_2 and H_2O on BP surface and matching output and input voltages can be obtained. Therefore, further work still needs to be done for an optimized gain and matched input and output voltages.

In summary, capping the BP FET with a layer of cross-linked PMMA introduces interfacial charges that converts the hole-dominated conduction to electron-dominated conduction. Combining the capped and pure BP FETs, a family of novel planar devices can be created, including BP-gated diodes, BP barristors, and BP logic inverters. These devices are potentially useful in digital electronic circuits that require current rectification, switching, and inversion. Moreover, these devices have the capability of lateral scaling due to the formation of a potential barrier in the vertical direction and provide a promising route for development of future 2D electronics.

Methods. The BP crystal was synthesized under high-pressure and high-temperature conditions with red phosphorus as a starting material, as previously reported.[42] BP flakes with thickness of around 10 nm were mechanically exfoliated using a Scotch tape method onto p++ Si substrates with a thermal oxidized SiO_2 layer of 100 or 300 nm. To minimize the atmospheric exposure, the exfoliation process is performed in a glovebox. To protect the BP flakes from degrading in atmospheric conditions, after exfoliation, the substrate is spin coated with a layer of PMMA (495, 2% in anisole) before being taken out for e-beam lithography. The thickness of the BP flakes was determined by a combination of atomic force microscopy and optical contrast, also verified by Raman spectrum characterization. The devices were fabricated using a standard e-beam lithography technique, followed by thermal evaporation of Cr/Au or Ni/Au (thickness 5/60 nm) metal stacks as contact electrodes (Supporting Information Figure S1). All measurements were performed in a vacuum chamber with vacuum level better than 10^{-6} Torr at room temperature and the electrical transport data were recorded by a Keithley 4200 SCS system and Agilent 4156 A.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b02704.

Detailed fabrication process of BP devices, Raman and AFM characterization of BP flakes, Schottky barrier reduction by capping with cross-linked PMMA in BP FETs, extraction of carrier mobility, tuning the introduced charges by varying dosage of electron beam, Raman characterization of original and cross-linked PMMA, determination of ideality factor of the BP diode based on the Schockley equation (PDF)

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Author Contributions

G.W. and L.B. contributed equally to this work. H.-J.G. supervised the entire project. G.C.W. and L.H.B. fabricated the devices. G.C.W., L.H.B., T.F.P., and R.S.M. performed transport measurements. L.L.S. provided the black phosphorus crystal. G.Y.Z. partially provided the measurement facility. H.F.Y., J.J.L., and C.Z.G. provided the microfabrication facilities for device fabrication. S.X.D. provided theoretical support. G.C.W., L.H.B., S.T.P., and R.D.S. analyzed the data. L.H.B. drafted the manuscript in consultation with H.-J.G., S.X.D., S.T.P, and R.D.S. All authors edited the manuscript.

Notes

The authors declare no competing financial interest.

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