Mass Production of Nanogap Electrodes toward Robust Resistive Random Access Memory

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Compared to volatile memory, nonvolatile memory (NVM) can memorize its state after the external voltage has been switched off, and has thus attracted lots of attention in the last decade. Being a dominant part of the semiconductor storage market, the performance of flash memory has improved significantly in the past, yet suffers from severe disadvantages during further scaling down.[1,2] Among various candidates to replace current flash memory, to continue the scaling trend toward ultrahigh-density storage, ferroelectric random access memory (FeRAM) shows the advantages of ultralow power consumption and an excellent endurance. However, the ferroelectric material in FeRAM will lose its essential ferroelectric characteristic at very small thicknesses, forbidding its application in ultrahigh-density storage.[2] Magnetic RAM shows ultrafast speed and extremely high endurance, yet suffers from high power consumption and is more prone to thermal noise when further scaling down.[2] Compared to other candidates, resistive random access memory (RRAM) based on the phenomenon of resistive switching (RS) has attracted considerable attention, showing great potential in meeting the demands of the ultimate nonvolatile data memory,[1] such as high access speed, low energy consumption, high performance with respect to endurance and retention, and ease of fabrication.[3] The general device configuration of a resistive-switching memory cell in an RRAM is a capacitor-like structure (metal–insulator–metal),[1] where the insulator layer can be made conductive (low resistive state (LRS)) through the formation of conductive filaments (CFs) after a "SET" operation, and restore to insulating state (high resistive state (HRS)), with a "RESET" operation. However, RS behavior can be classified into two modes: NVM switching (MS) and volatile threshold switching (TS), and studies have shown that the two modes can coexist in a single device.[4,5] Between the two modes of the RS behavior, only the MS mode can be used for nonvolatile data storage, in which the LRS and HRS can be maintained after removing the external voltage.[4] On the contrary, in the other mode, TS, the LRS cannot be maintained once the applied voltage is removed. Hence, it is of great importance to control the RS modes to be the MS mode for the application of RRAM.

Recently, Sun et al. demonstrated that the CF morphology determines the working mode. Specifically, the formation and dissolution of CF, consisting of continuous nanocrystals, is the mechanism behind the MS mode, while TS originates from discontinuous CF with isolated nanocrystals.[4] Their result is of great significance, in that it gives us a clue that if we shrink the distance between the two metal electrodes to the nanometer scale, continuous CF can be formed more easily under an applied electrical field. Apart from increasing the occurring rate of the MS mode, a nanometer-scale distance between two metal electrodes, also known as nanogap electrodes, shows potential to bring about other benefits.[6] First, with the key component on the nanometer scale, the size of each cell can be greatly reduced, which is crucial in realizing ultrahigh-density storage. Secondly, the operation voltage can be reduced by using nanometer-scale structures, which is beneficial in reducing energy consumption. Moreover, the time required for the formation of the CFs can also be minimized with nanometer distances,[7] which is beneficial in realizing a high access speed. Up to now, a few studies have shown the performance of nanogap electrodes as a nonvolatile resistive switch,[7–11] yet there is a long way in front of us before the application of nanogap electrodes in ultrahigh-density storage, especially, mass production of nanogap electrodes and performance improvement.

In the past decades, a variety of techniques for the fabrication of nanogap electrodes have been developed.[12] Some of the techniques require expensive equipment, such as electron-beam lithography (EBL),[13,14] transmission electron microscopy,[15] focused ion beam (FIB),[16] molecular-beam epitaxy,[17] etc., which is accompanied by high cost and lack the ability of mass production. Other techniques, including shadow evaporation,[18] lateral oxidation of metal,[19] on-wire lithography,[20] etc.,[21] have also been developed. Some of these techniques have demonstrated the ability of mass production. However, there remain some challenges encountering us; for example, short circuits can hardly be avoided in the fabrication of sub-10 nm gaps using shadow evaporation. A lot of important results have been demonstrated using on-wire lithography,[22] yet it requires extra steps such as lithography to connect the wire to the outer

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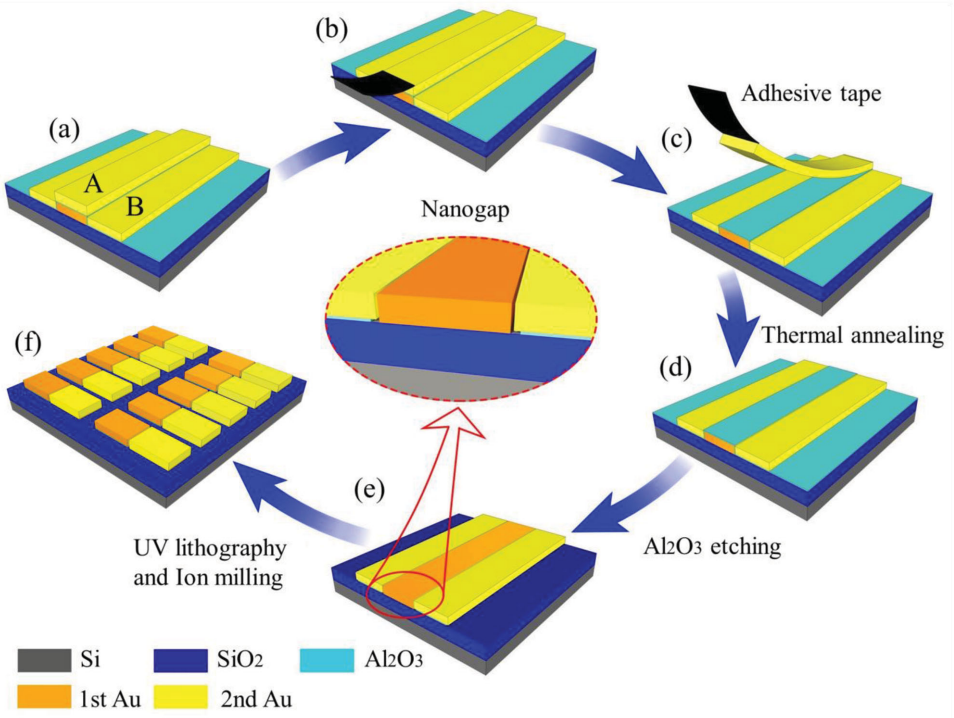

Figure 1. Illustration of the fabrication process of nanogap electrode arrays: a) Schematic diagram of the Au/Al_2O_3/Au structure. b,c) The removal process of part A of the second-layer Au through an adhesive tape (in black): the removal process began at one end of the stripe and processed slowly to the other end until the whole stripe was removed completely. d) The TA process was used to smooth part B of the second-layer Au. e) The formation of the nanogap between the first- and second-layer Au through the removal of Al_2O_3 by chemical etching. An enlarged view of the structures obtained was illustrated in the middle. f) Nanogap electrodes arrays fabricated through UV lithography and ion milling.

circuit for measurement. Hence, a new method for mass production of nanogap electrodes is needed for the application in RRAM.

Recently, atomic layer deposition (ALD) has become a popular tool in the production of optical nanogap arrays, not only because of the atomic-scale resolution, but also the conformal nature of the deposited Al_2O_3 film.[23–26] Combined with adhesive tape or ion milling techniques, the nanogaps obtained have demonstrated application in optics, such as surface-enhanced Raman scattering and surface-enhanced infrared absorption spectroscopy.[24,25] Here, we take a step further and show that, by a refined method, electrical nanogap electrodes arrays can be fabricated in mass production, which can be used in nonvolatile resistive switches.

The fabrication process of nanogap electrodes is illustrated in **Figure 1**. The process begins with structures shown in Figure 1a. First, UV lithography was adopted to pattern a double-layer resistance of LOR 5A/S1813 on 500 nm SiO_2/Si substrate into stripes about 1 mm in width, so that after the metal deposition (5 nm Cr/150 nm Au) and lift-off process, metal stripes with a vertical sidewall can be obtained. Second, ALD (at 250 °C) and thermal evaporation were used in sequence to cover the whole surface of the substrate with 5 nm Al_2O_3 and 150 nm Au respectively. The second layer Au can be divided into two parts (A and B). Part A is above the first layer Au and Al_2O_3, while B is the part left over, as illustrated in Figure 1a. The above-mentioned process is similar to other reports,[25,26] with the main difference lying in the size and shape of the patterns. However, such methods required a following anisotropic ion milling,[25] which resulted in not only the removal of part A, but also most of part B, impeding its application in electronics such as molecular electronics. Simultaneously, part A was removed by gently contacting it with one-sided Scotch tape and peeling it off.[26] Here a similar but revised process to that described by Chen et al.[26] was used to remove part A. Specifically, a piece of adhesive tape with width around 1 mm was put into contact with one end of part A stripe and began to move slowly to the other end until the stripe separated from the substrate completely, as showed in Figure 1b,c. Since the second Au film with thickness of 150 nm is strong enough and the adhesive to the Al_2O_3 layer is weak, the whole Au stripe (part A) can be removed over a length as long as several centimeters without any residual being left. By this step, a structure of Au (first layer)/Al_2O_3/Au (part B in second layer) was formed in the plane of the substrate. Next, thermal annealing (TA) at 500 °C for 5 min in a N_2 atmosphere was carried out to smooth the edge of the second layer Au left over. The Al_2O_3 was then removed by an etching agent of a mixed solution of H_3PO_4 and H_2SO_4 (volume ration of 1:3) at 260 °C for 40 s, and rinsed in deionized water after the substrate was cooled to room temperature. After removal of the Al_2O_3, a nanogap between the first layer stripe and the second layer stripe was obtained, as shown in Figure 1e. Then, one more patterning technique can be used for the fabrication of nanogap electrodes with various aspect ratios. Here, two different processes are demonstrated to pattern the structures in Figure 1e

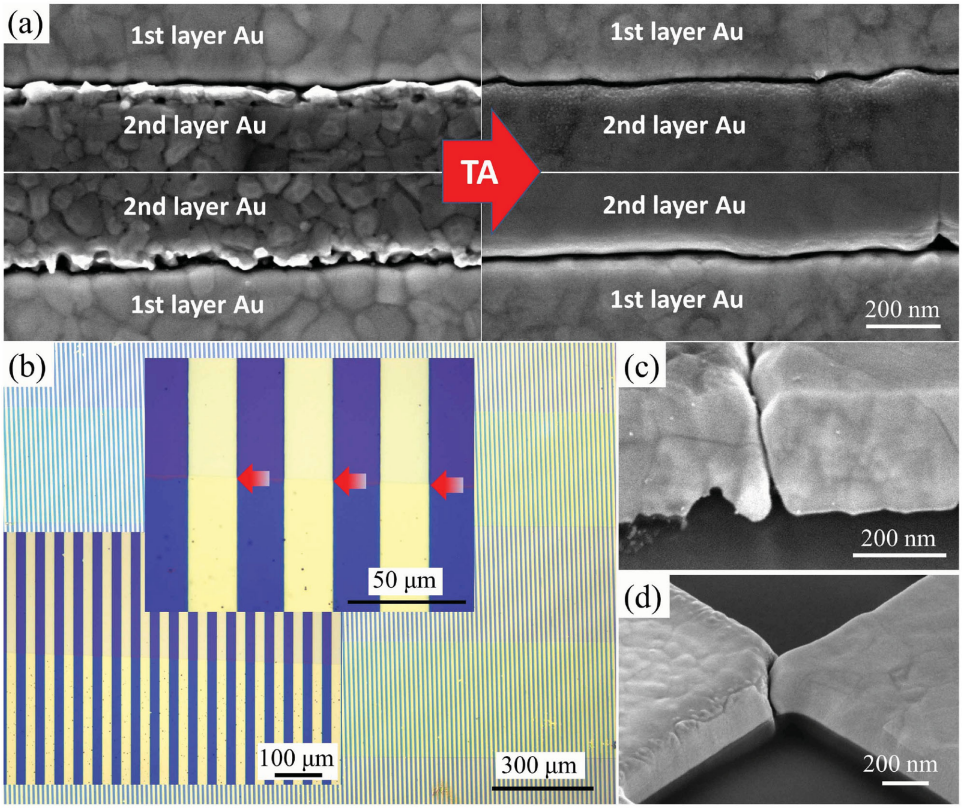

Figure 2. a) SEM images (top view) of the as-fabricated Au/Al_2O_3/Au and that after a thermal process in N_2 under 500 °C for 5 min, showing the smooth edge of the second-layer Au after TA. b) Optical image of the nanogap electrodes arrays with different magnifications, the red arrow indicates the location of the nanogap. c) SEM image of the sidewall of the nanogap electrodes. d) SEM image of nanogap electrodes with small aspect ratio fabricated with FIB milling. (c) and (d) were taken with the incident angle of the electron beam equal to 45°.

into nanogap electrodes in Figure 1f, either the combination of UV-lithography and ion milling, or just FIB milling. UV lithography and ion-milling techniques were combined to pattern the structures into nanogap electrodes arrays with a large aspect ratio, and hundreds, even thousands of nanogap electrodes can be fabricated at the same time. FIB was used for the fabrication of nanogap electrodes with a smaller aspect ratio. In the end, an oxygen plasma process was performed to clean the whole sample thoroughly.

One crucial step in obtaining the nanogap electrodes arrays is TA. As can be seen from the images on the left of **Figure 2**a, which correspond to the structure obtained after the step shown in Figure 1c, after removing part A of the second layer Au, the edge of the left B part was bumpy with protrusions and hollows along the whole edge. Such protrusions and hollows are detrimental, especially for electrical nanogaps, because they would cause size variations or even short circuits between the first layer Au and second layer Au. Here a TA process was adopted to improve the situation. The TA temperature is very important considering the thermal dewetting properties of Au on Al_2O_3, in that a lower temperature is not enough to smooth the bumpy edge, and a higher temperature such as 700 °C can result in a huge morphology change, which turns the Au film into many separated grains. Here, a TA process of 500 °C for 5 min in N_2 atmosphere was used, after which the edge of the second layer Au becomes smooth because of thermally induced recrystallization and thermal dewetting of Au on Al_2O_3.[27] As shown in the right-hand images in Figure 2a, which correspond to the structure in Figure 1d, the bumps along the edge disappeared and a uniform nanogap of Al_2O_3 was obtained after the TA process. Figure 2b shows an optical image of parts of the fabricated nanogap electrodes array, which corresponds to Figure 1f. As can be seen from the inset, there is a slight color difference between the first layer Au and the second layer Au, which can be used to distinguish the location of the nanogaps. The red arrows in Figure 2b indicate the location of the nanogaps. Figure 2c shows a scanning electron microscopy (SEM) image of the sidewall of the fabricated nanogap electrodes, demonstrating a clear uniform nanogap, indicating the successful fabrication of the nanogap electrodes arrays. Nanogap electrodes with a smaller aspect ratio, fabricated by FIB milling, are demonstrated in Figure 2d.

The electrical properties of the obtained nanogap electrodes as resistive-switch memory cells were studied in vacuum under a base pressure of ≈10^{-2} Pa at room temperature using a semiconductor characterization system (Keithley 4200-SCS). The nanogap electrodes under measurement are those shown in **Figure 3**a, with an aspect ratio of more than several thousands (length:width = 40 μm:≈5 nm), which is beneficial in avoiding nonuniformity-related effects. Figure 3b shows a typical *I*–*V* curve of the device with initial HRS under a current compliance (I_c) of 1 mA. By sweeping from 0 to 15 V and 15 to 0 V

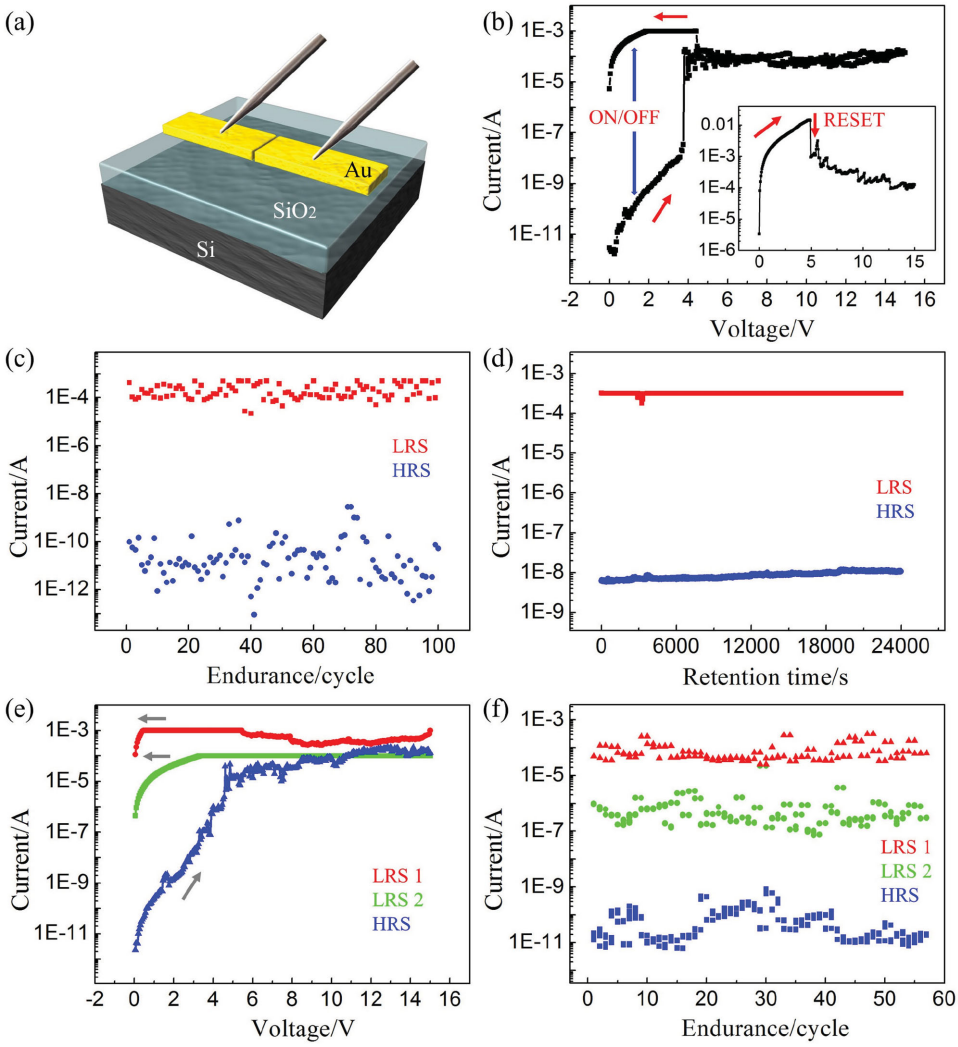

Figure 3. a) Schematic of a resistive switch based on nanogap electrodes. b) *I–V* curve of nanogap electrodes with initial HRS by sweeping from 0 to 15 V and 15 to 0 V, showing typical unipolar resistive switching behavior. The inset shows the *I–V* curve with initial LRS by sweeping from 0 to 15 V, showing a RESET around 5 V. c) Repetitive resistive switching characteristics of the nanogap electrodes; the resistance was READ under 0.5 V. d) Retention of ON/OFF states of the device. e) *I–V* curve of nanogap electrodes under two different values of I_c (0.1 and 1 mA) by sweeping from 15 to 0 V. f) Repetitive resistive-switching characteristics under two different values of I_c, showing 3-bit storage ability.

continuously, a typical and stable unipolar switching behavior can be identified. LRS is commonly used as the ON state and HRS as the OFF state; thus, the terms of ON and OFF will be used in the text below. In a forward sweep from 0 to 15 V, the device begins with an OFF state below 4 V. In the backward sweep (15 to 0 V), it jumps from an OFF state to an ON state and keeps the ON state below 4 V, producing a current hysteresis in the bias range of 0–4 V with a high ON/OFF ratio of ≈10^4. "SET" is defined as the operation to switch the device from the OFF state to the ON state and "RESET" is defined as the operation to switch the device from the ON state to the OFF state. Here, a RESET voltage can be observed at around 5 V when applying a voltage sweep from 0 to 15 V for initial ON devices, as shown in the inset of Figure 3b. Figure 3c shows the memory effect of the device. The resistances shown in Figure 3c were measured under a READ voltage of 0.5 V, showing an ON/OFF ratio of about 10^4, demonstrating the nondestructive memory property. Figure 3d shows data retention in a continuous READ process at 0.5 V, and an ON/OFF ratio of ≈10^4 was maintained for more than 2×10^4 s without obvious degradation. The ability of multibit storage was also explored with different I_c. As can be seen from Figure 3e, after sweeping from 15 to 0 V under two different I_c (0.1 and 1 mA), the resistance shows different values at a READ voltage 0.5 V. Figure 3f shows repetitive resistive-switching characteristics under the two different values of I_c, showing stable 3-bit storage ability over more than 50 cycles, implying a great potential of the structure in multibit storage. More than 60% of devices present a similar nonvolatile resistive-switching behavior, with SET voltage varying among 3.0 ± 2.0 V from device to device and an ON/OFF ratio larger than 10^3. The observation confirmed that the nanogap electrodes can function as an RRAM cell.

The mechanism of the nonvolatile resistive switching behavior can be generally explained as the formation and

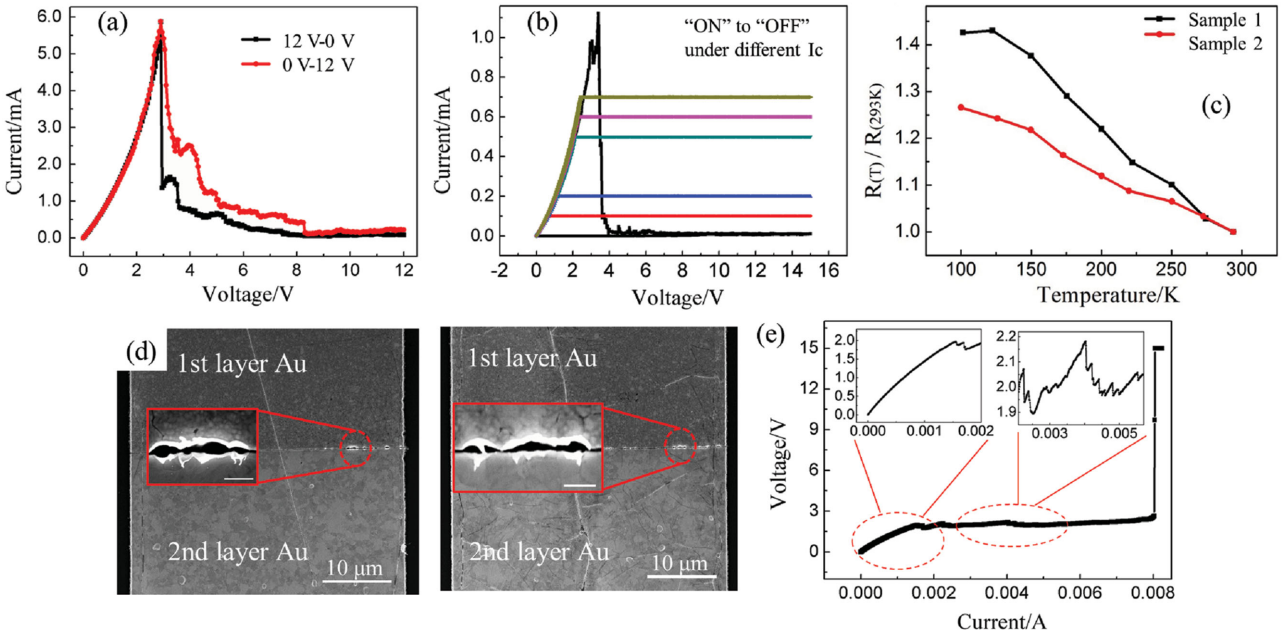

Figure 4. a) *I–V* curves of one device by sweeping from 12 to 0 V and 0 to 12 V, respectively, showing the same I_{max} value. b) *I–V* curve of one device by sweeping from 0 to 15 V under different values of I_c (smaller than I_{max}) after switching ON by sweeping from 15 to 0 V (black), showing no switching from ON to OFF. c) Normalized resistances $R_{(T)}/R_{(293K)}$ as a function of temperature for two different samples, showing increased resistance upon the decrease of the temperature. d) SEM images of the nanogap electrodes after several switching cycles, demonstrating damage in the nanogap region. e) *I–V* curve of one device with initial ON state under current sweeping, showing a further SET process, reaching another ON state with a smaller resistance.

dissolution of CFs. In our case (Au nanogap electrodes on SiO_2/Si substrate), specifically, two kinds of CFs might contribute to the nonvolatile storage behavior. On the one hand, metal atoms in an electrical field suffer from two forces, a direct electrostatic force F_e and a force F_p from the exchange of momentum with other charge carriers such as electrons. The direct electrostatic force F_e drives the metal ions to move along the direction of the electrical field and leads to the formation of metallic CFs, also known as field-emission-induced electromigration, which has been proved by a series of reports and by fundamental theory.[8,28,29] The force F_p induced by a so-called "electron wind" causing the metal atoms to move along the flow of the electrons is the mechanism behind the dissolution of CFs, which has become one of the most frequently used methods for the fabrication of nanogap electrodes, known as electromigration.[14,30] On the other hand, it has been demonstrated by Yao et al. that, instead of being a passive, insulating component in electronic devices, reversible reduction and oxidation of silicon (Si) nanocrystals (NCs) in a SiO_2 substrate can give rise to nonvolatile resistive-switching properties.[31,32] Specifically, a voltage-driven electrochemical process can take place and induce local reduction of SiO_x into Si, which can aggregate into Si NCs under the help of the generated heat in the process. The formation of the Si NCs pathways leads to increased conductance and a switching from HRS to LRS. Thermal rupture of Si CFs, driven by current induced local heating, is thought to be the reason for the transition from LRS to HRS, exhibiting a typical unipolar switching behavior. The similar value between the electrical field, to drive the migration of Au atoms and to cause the SiO_2 breakdown induced filaments, makes the mechanism a little complex; thus, this needs to be explored further.

In order to figure out the exact switching mechanism of the device, further device characterization was carried out and several phenomena were observed. First, a sweeping from 12 to 0 V will always result in the ON state, as can be seen from **Figure 4**a, in which the black curve reaches a maximum current (I_{max}) of about 5.5 mA through a sudden jump and then reduces smoothly to zero as the voltage approaches 0 V, keeping the ON state. When a voltage sweep from 0 to 12 V was conducted next, a switch from ON to OFF was shown around 5.5 mA, as shown by the red line of Figure 4a, showing almost the same I_{max} with the OFF to ON curve. Second, after switching a device to the ON state by sweeping the voltage from 15 to 0 V, a different I_c was applied when sweeping from 0 to 15 V. As can be seen from Figure 4b, as long as the I_c is smaller than I_{max}, the devices maintain the ON state without switching to OFF. Third, the device shows a very stable and repeatable performance in vacuum, which can hardly be observed in ambient air. Fourth, the resistance of an ON-state device increases with the decrease of the temperature, as shown in Figure 4c. Fifth, the resistive-switching behavior disappears when the temperature is lower than 100 K, such that under a low temperature, the devices can show a switch from LRS to HRS; however, a reversed switch from HRS to LRS cannot be realized. Moreover, breakdown-induced damage in the nanogap region can be observed for almost every device after switching cycles, as shown in Figure 4d.

From the first two phenomena, a conclusion can hardly be drawn, because the two kinds of CFs can both show similar behavior. However, the remaining phenomena indicate that Si

CFs play a more important role in the device, causing the resistive-switching behavior. First, the device was unable to be SET from HRS to LRS in air, which is a sign of the Si CFs mechanism, because an oxygen environment hinders the reduction of the SiO_2 to Si, thus forbidding the formation of Si CFs.[31] Second, the resistance of the ON-state device increases with the decrease of the temperature, which confirms the existence of Si CFs; otherwise, the resistance of the ON-state device will decrease with the decrease of temperature, which is typical for a metal. The reason behind the fifth phenomenon was that the formation of Si CFs is not only electric field driven but also thermally related, in that local heating was necessary for the aggregation of Si into Si NCs and Si CFs.[31] Consequently, under low temperature, the devices cannot be switched from HRS to LRS. Moreover, damage to the SiO_x substrate in the nanogap region is typical for resistive switches, behind which the switch is caused by the formation and dissolution of Si CFs.[31,32]

At this stage, we have identified the formation and dissolution of Si CFs as the main mechanism of the resistive-switching behavior. However, we cannot rule out the migration of Au atoms and its contribution to the performance of the device. Reports on nanogap electrodes fabricated through a nondestructive way such as EBL or shadow-mask techniques have also demonstrated the behavior of resistive switching, and the mechanism was attributed to the migration of metal atoms, in which the electric fields required to trigger the migration of metal atoms and related switching are around MV cm^{-1},[7–11,33] agreeing with the reported value obtained through the other way.[34] Since the electric field to trigger the switch is about the same order of magnitude here, migration of Au atoms can also take place in the process and can contribute to the conductance by either shrinking the gap width or forming a few CFs.

In addition, the mechanism behind the multibit-storage ability was further explored using a new method reported recently,[35] in which a current sweep mode instead of the voltage sweep mode used above was adopted to explore the process. For an initial ON-state device that was SET under an I_c, no resistance reduction in the current range from 0 to 1.5 mA can be observed on the *I*–*V* curve shown in Figure 4e. After that, dozens of voltage peaks and valleys appeared continuously till the RESET process set in. Each peak-to-valley transition means a resistance decrease corresponding to the formation of new CFs or CF growth between the two electrodes. The additional decrease in resistance is equal to another SET process, reaching another ON state with smaller resistance. Hence, with continuous formation of CFs, lots of discrete resistance states can be reached, explaining the ability of multibit storage.

In conclusion, a method in which ALD, adhesive tape, and chemical etching are combined, is demonstrated here for mass production of nanogap electrodes arrays with gap width predetermined by the thickness of ALD-deposited Al_2O_3 with sub-nanometer resolution. A unipolar nonvolatile resistive switching behavior was identified in the obtained nanogap electrodes, showing stable, robust performance and the ability of multibit storage, demonstrating great potential in ultrahigh-density storage. The formation and dissolution of Si CFs and migration of Au atoms is the mechanism behind the resistive switching.

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