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Dual-gate field effect transistor based on ZnO nanowire with high-K gate dielectrics

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ABSTRACT

Dual gate ZnO nanowire field-effect transistor (FET) with high-k Al_2O_3 or HfO_2 gate dielectrics was configured, which shows good transistor performance with a high on/off ratio ($\sim 10^4$), a low operation voltage (below 1 V), a high peak transconductance (7.5 nS), a relatively high field effect mobility (0.27 $cm^2/V{\cdot}s$) and ultralow leakage current ($\sim 10^{-13}$ A). These results indicated that the ZnO nanowire FET in top-gate mode provided a better device performance than that in bottom-gate mode. Moreover, the effects of Al_2O_3 and HfO_2 gate dielectric layers on enhancing the FET performance were discussed.

1. Introduction

As an one-dimension semiconductor materials, ZnO nanowires have attracted intensively interest and are becoming a prime candidate due to their special material properties and wide-ranging device application in the field of electronic and optoelectronic [1]. As one of the elementary building blocks of nanoelectronic devices, field–effect transistors (FETs) based on nanowires have been shown to operate at ultralow power below microwatts with enhanced operation speed [2]. Therefore, the ZnO nanowires FET attract a great deal attention on the electrical characteristics and the configuration [3–6].

Most of previous reports about ZnO nanowire FETs have focused on the bottom-gate configuration with SiO_2 as a dielectric layer [7], however, their weak dependence on the gate voltage demands higher voltage and thinner SiO_2 dielectric, which will lead to a considerable increase of leakage current due to the quantum-mechanical tunneling effect through the thin dielectric layer [8]. Therefore, some high-k dielectric materials were used in the FETs to ease the demand on the thickness of dielectric layer and avoid inducing high leakage current and causing dielectric breakdown. On the other hand, the top-gate FETs were also configured, which are more desirable for integrated circuit fabrication [9]. However, the dual-gate operating in one FET devices with high-k dielectric layer as a gate insulator layer has been rarely reported so far.

In this paper, a dual-gate ZnO nanowire field effect transistor device on Si substrate has been fabricated. The electrical characteristics of dual-gate single ZnO nanowire FET with Al_2O_3 or HfO_2 dielectric layer by atomic layer deposition (ALD) have been studied. Here ALD technique adopted is a promising deposition method with many advantages in excellent conformity, uniformity and good compactness with low impurity. We also drew a comparison between the performance of FET device with top-gate mode and bottom-gate mode. Moreover; the different effects of Al_2O_3 and HfO_2 gate dielectric layer on the electrical characteristics of ZnO nanowire FETs have been discussed.

2. Experimental details

Firstly, we used single-crystalline ZnO nanowires as the channel of the FET devices, which were grown using Zn particle and C powders in a hot-wall CVD system on Si substrate coated with 50 nm Au film as catalyst. The general synthesis method and growth mechanism have been elaborated elsewhere [10,11]. Fig. 1 shows a scanning electron microscope (SEM) image of as-grown ZnO nanowires before ultrasonic dispersion. For the fabrication of the nanowire-based FETs in this work, some individual ZnO nanowires with a diameter in a range from 100 to 120 nm were chosen. Their average length is 8 μm with circular cross section.

Secondly, the as-grown ZnO nanowires were dispersed in isopropyl alcohol and then spin-coated onto a heavily doped *p*-Si substrate coated by 50 nm high-k dielectric layer (Al_2O_3 or HfO_2) as insulator layer. This substrate would be served as a bottom-gate electrode in the FETs. After mapping a single ZnO nanowire by SEM, the source and drain electrodes with Au/Ti layers (150/5 nm) were formed on both ends of a single nanowire by electron beam lithography and thermal evaporation deposition, followed by a lift-off process. After that, a 20 nm dielectric layer was deposited conformably on the substrate as well as the ZnO nanowire channel by atomic layer deposition method (ALD). It is noted that the ZnO nanowire channel is surrounded by the thin film avoiding to be damaged in the procedure of device fabrication. During the ALD process, the same temperature (250 °C) and pressure (260 mtorr) are kept for high-quality Al_2O_3 and HfO_2 gate dielectric layer deposition. Finally, the same steps including electron beam lithog-

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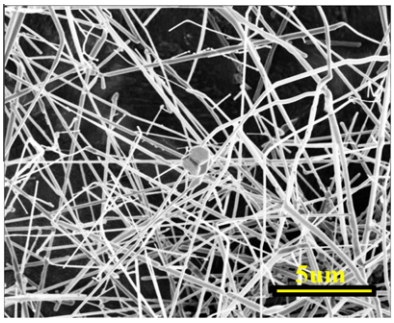

Fig. 1. SEM image of ZnO nanowires.

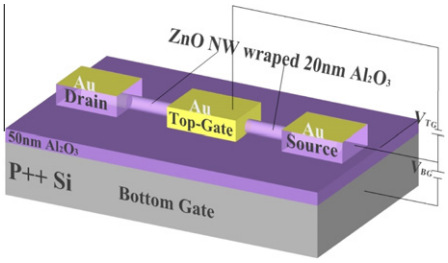

Fig. 2. The schematic diagram of dual-gate FET.

raphy, thermal evaporation deposition and lift-off process was carried out for a fabrication of top-gate electrode at the center of the ZnO nanowire. Additionally, it is noticeable that the dielectric layer is also deposited on the source and drain electrodes during the ALD process. Therefore, to expose the source and drain contact pads buried in the dielectric layer, a reactive ion etching (RIE) for the dielectric layers were carried out. Although the dielectric layer wrapped in ZnO nanowire and the top-gate electrode will also be etched, the dielectric layer underneath the top-gate cannot be removed. In order to etch completely the dielectric layer covered over the source and drain electrodes, the top-gate electrode should be deposited a thicker layer of Au film due to the low selectivity between the gold film and dielectric layer.

By above microfabrication processes, a dual-gate ZnO nanowire FET device can be configured. Fig. 2 shows a schematic illustration of the dual-gate ZnO nanowire FET with heavily doped *p*-Si bottom-gate and Au top-gate. Device performance of this dual-gate FET was characterized using a probe stage equipped with semiconductor characterization system (keithley 4200) in an ambient enviroment (at room temperature in air and without illumination).

3. Results and discussion

The top-view SEM image of an integral dual-gate ZnO nanowire FET is shown in Fig. 3. The single ZnO nanowire is 8 μm in length, 80 nm in diameter and the source-drain electrode is 1 μm in width at both ends of nanowire and the top-gate electrode is 2 μm in width in the middle.

The top-gate and bottom gate FETs are fabricated in one device in our work, prior to the characterization of top-gate FETs, a typical output and transfer characteristics obtained from bottom gate ZnO nanowire-based FET are showed in Fig. 4. The group of I_{ds}–V_{ds} curves in Fig. 4a shows that the drain current (I_{ds}) increases with drain voltage (V_{ds}) with a fixed gate voltage, and the slopes of the I_{ds}–V_{ds} curves are dependent on the gate voltage. A typical I_{ds}–V_{gs} curve obtained from the bottom-gate FET at a V_{ds} of 5 V is

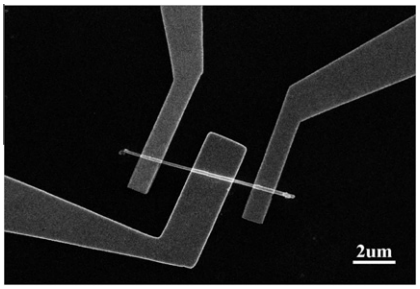

Fig. 3. SEM image of ZnO nanowire FET.

plotted in Fig. 4b. The current carrier depletion was observed at a V_{ds} of −2 V, and its I_{on}/I_{off} ratio is close to 10^3. Its peak transconductance ($g_m = dI_{ds}/dV_{gs}$) is roughly estimated to be ~2.65 nS when V_{ds}, V_{gs} is 5 V, −3.5 V, respectively. The oxide capacitance of the bottom-gate FET was obtained to be 18.2 fF from the equation, $C_{ox} = 2\pi\varepsilon_r\varepsilon_0 L/\ln(2h/r_{nw})$ [12], where ε_r is the dielectric constant of Al_2O_3 (~9) and L is the gate length (8 μm); h and r_{nw} is the thickness of SiO_2 (50 nm) and the radius of the nanowire (80 nm), respectively. Additionally, the field effect mobility was estimated to be 0.093 $cm^2/V{\cdot}s$ on the basis of the formula: $\mu_{FE} = L^2 g_m/C_{ox}V_{ds}$ [12].

The electrical characteristics of the top-gate ZnO nanowire FET are shown in Fig. 5. Fig. 5a shows typical I_{ds}–V_{ds} characteristic curves obtained at V_{gs} values ranging from 0 to 1 V with a step of 0.5 V in top-gate mode operation. The I_{ds}, increases with increasing V_{ds} and becomes smaller when larger positive V_{gs} is applied, which indicates a *p*-type semiconduting [13]. Moreover, we found that the top-gate mode operation of ZnO nanowire FET exhibited a lower V_{gs} values to regulate the same amplitude of I_{ds} than bottom-gate mode operation. In the I_{ds}–V_{gs} curve plotted in the Fig. 5b, the drain current (I_{ds}) of the top-gate FET decreases as the gate voltage is swept from −4 to 4 V at V_{ds} values ranging from −1 to 2 V with a step of 1 V. Also, the channel of the top-gate ZnO nanowire FET could be fully depleted at V_{ds} values ranging from −1 to 2 V. As a result, FETs' peak transconductance (g_m) is 7.5 nS at $V_{gs} = -2.05$ V and $V_{ds} = -1$ V, and the I_{on}/I_{off} ratio at $V_{ds} = 1$ V is close to 10^4, which is larger one order of magnitude than that of bottom mode operation of the FET. From the Fig. 5b, it is cleared noted that the threshold voltage V_T in top-gate mode operation is determined to be −2.5, -0.5, 0.5, and 1.5 V at $V_{ds} = -1$, 0, 1, and 2 V, respectively. These results indicated that V_T was shifted from a negative gate voltage to a positive gate voltage, which corresponded well with previous reports on ZnO nanowire-based FETs [14,15]. This V_T shifting to positive gate bias mainly results from a surface depletion induced channel narrowing effect owing to the existence of an electron trap in the ZnO nanowire. The oxide capacitance of the top-gate FET was found to be 4.55 fF from the equation, $C_{ox} = 2\varepsilon_r\varepsilon_0 L_g/\ln(r_g/r_{nw})$, [12] where L_g is the gate length (2 μm) and r_g is the outer radius of the Al_2O_3-coated nanowire (100 nm), and r_{nw} is the radius of the nanowire (80 nm). The field effect mobility was estimated to be 0.272 $cm^2/V{\cdot}s$ on the basis of the formula, $\mu_{FE} = L_c L_g g_m r_g/C_{ox}V_{ds}r_{nw}$, where L_c is channel length between source and drain. It is cleared the field effect mobility of FET in top-gate mode is roughly 3 times larger than that of FET in bottom-gate mode. These results revealed that the top-gate mode of ZnO nanowire FET exhibited better performance than the bottom-gate mode, which is mainly attributed to strong electrostatic gating in top-gate mode FETs [9]. Another factor refer to the better characteristics in top-gate mode is the thickness of the gate dielectric layer. The thinner gate dielectric layer thickness (20 nm) in top-gate mode FET, compared with gate dielectric layer thickness (50 nm) in bottom-gate mode FET, is very favorable to

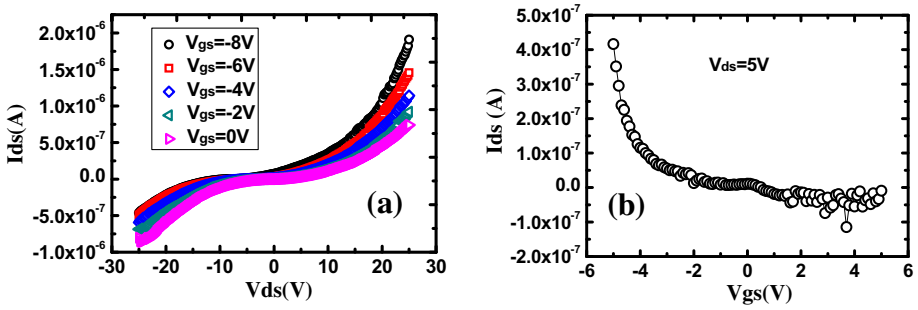

Fig. 4. The typical output (a) and transfer (b) characteristics obtained from the ZnO nanowire-based bottom-gate FET with Al_2O_3 film as dielectric layer.

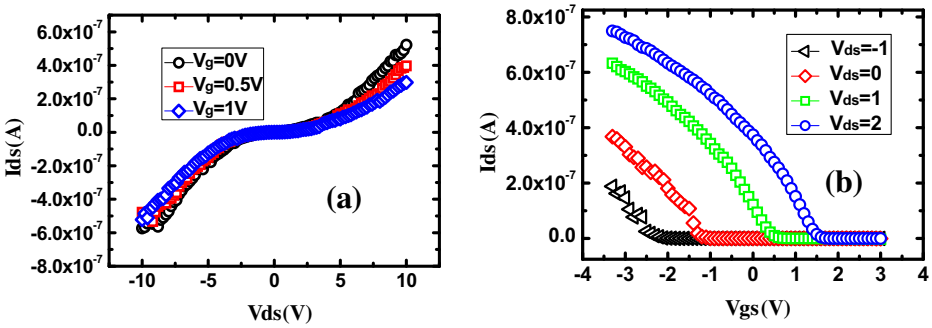

Fig. 5. The output (a) and transfer (b) characteristics obtained from ZnO nanowire-based top-gate FET with Al_2O_3 film as dielectric layer.

generating a higher value of transconductance, more effective on–off current control and higher field effect mobility.

Generally speaking, it is expected that the FET with high-k dielectic layer HfO_2 film would exhibit better FET performance due to its higher dielectric constant reaching to ~20 than Al_2O_3 film. However, our measurement results show that when Al_2O_3 dielectric layer is replaced by HfO_2 film, the output and transfer characteristic of FET has not an obvious change. The possible reason would be that the HfO_2 film surface topography properties worsen the performance of FET. Although the HfO_2 film has a larger dielectric constant, its surface topography is inferior to that of Al_2O_3 film at the same ALD condition, the occurrence of micro-crystal during the HfO_2 growth process and the interface effect between ZnO nanowire and HfO_2 would be other factors for no improvement performance compared with FETs adopting Al_2O_3 film [16].

In addition, the leakage current characteristics of the Al_2O_3 and HfO_2 dielectric film between the gate metal and the nanowire channel was measured as a function of V_{gs} from 0 to 5 V, without applying V_{ds}, as shown in Fig. 6. It is very obvious that leakage current of HfO_2 film is far higher than that of Al_2O_3 film, and this trend increases gradually with enhanced V_{gs}. When V_{gs} is increased to 5 V, the leakage current of Al_2O_3 film varied from 0 to 0.15 pA while the leakage current of HfO_2 film varied from 0 to 1.5 pA. At a gate voltage of 5 V, the leakage current of HfO_2 is one order of magnitude larger than that of Al_2O_3 film, which would directly affect the performance of FET. Nevertheless, these magnitudes of the leakage current are small enough to function as gate oxide layer. This small leakage current reveals that high-k dielectric layers including Al_2O_3 and HfO_2 film are practically very useful as a gate material in the fabrication of nanowire-based FETs.

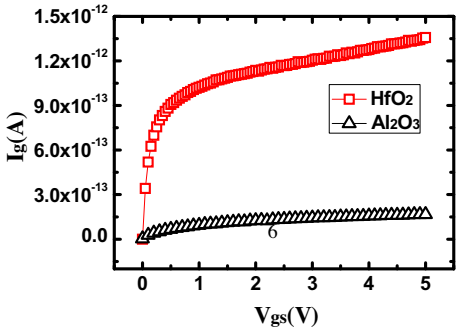

Fig. 6. Leakage current of Al_2O_3 (triangle) and HfO_2 (square) gate material between the gate metal and the nanowire channel measured for top-gate FET as a function of the gate voltage.

4. Conclusion

We have fabricated the dual-gate ZnO nanowire-based field effect transistor. The electrical characteristics of this ZnO nanowire-based FET have been investigated in bottom-gate mode and top-gate mode, respectively. The top-gate configuration FET can be performed at a lower gate voltage, higher on-off ratio and field effect mobility than that of bottom-gate. To sum up, the current on/off ratio of bottom-gate mode and top-gate mode of FET is 10^3 and 10^4, the peak transconductance is 2.65 and 7.5 nS, and the field effect mobility is 0.093 and 0.27 $cm^2/V{\cdot}s$, respectively. The results above are superior to some literatures using SiO_2 film as dielectric layer. In addition, Al_2O_3 showed a lower leakage current than HfO_2 as a gate dielectric layer, but both the Al_2O_3 and HfO_2 film are excellent insulator layers proved by the low leakage current for FET devices.

Acknowledgements

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