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Field effect transistors with layered two-dimensional SnS2−xSex conduction channels: Effects of selenium substitution
Few-layer SnSe₂ transistors with high on/off ratios

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Graphene’s success has triggered extensive research on isolation, characterization, and device applications of two-dimensional (2D) layered materials.¹ The successful isolation and synthesis of transition-metal dichalcogenide (TMD) atomic layers such as MoS₂ boosted the research on exploration of fundamentally interesting physical phenomena and technological applications in electronics and optoelectronics benefitting from their sizeable and thickness-dependent bandgaps, which are not present in graphene.²,³ In TMDs, the d electrons are the main source to form lower valence band maxima, inducing a band transition from indirect to direct bandgap when reduced to single atomic layer.⁴ Consequently, strong photoluminescence properties are present in single-layer TMDs.²

Recently, the demonstration of few-layer SnS₂ for applications in transistors,⁻⁵ logic circuits, and photodetectors⁶ extends this system to dichalcogenides of metals from the main group in the periodic table of the elements. Compared to TMDs, no d electrons are involved in the bonding configuration of these metal dichalcogenides. As a result, new phenomena emerge. For example, the bandgap gets smaller for SnS₂ when reducing the thickness from bulk to monolayer, which is contrary to that of TMDs.⁷ As a close relative, few-layered SnSe₂ with similar band structure has been rarely investigated.⁸ Previous attempts on SnSe₂ field effect transistors (FETs) indicated that the current cannot be completely turned off due to the high electron density in SnSe₂ layers.⁹ In TMDs, the out-of-plane A₁g mode shows a blue shift with the relaxation of in-plane bonding.¹⁰ However, for SnSe₂, the thickness-dependent feature disappears when it is beyond five layers.¹¹²

In previous studies, a thickness-dependent Raman spectrum has been frequently observed in 2D TMDs materials, where the out-of-plane A₁g mode shows a blue shift with increasing thickness due to the stiffening of the out-of-plane phonons; on the other hand, the in-plane degenerate E₉ mode shows a red shift upon the addition of extra layers due to the relaxation of in-plane bonding.¹³ However, for SnSe₂ flakes with different thicknesses, the Raman spectra of the out-of-plane A₁g mode at 187 cm⁻¹ and in-plane E₉ mode at 112 cm⁻¹ do not show any thickness-dependent features, as shown in Figure 1(d). Similar to MoS₂, the thickness-dependent feature disappears when it is beyond five layers.¹⁴ In fact, there are two kinds of CdI₂-type stacking orders in SnSe₂ crystals, 1T and 6Hb polytypes.¹⁵,¹⁶ Both of their out-of-plane A₁g modes are located near 185 cm⁻¹ and in-plane...
The structure of SnSe$_2$ in our study can be identified as 1T, suggesting a low contact resistance.

The coincidence between two- and four-probe measurements are performed. As shown in Figure 2(b), a good linear relationship between the current and bias voltage indicates a good Ohmic contact between Cr/Au electrodes and the interface of SnSe$_2$. Moreover, the coincidence between two- and four-probe measurements suggests a low contact resistance.

SnSe$_2$ FETs are fabricated by a standard electron-beam lithography technique followed by deposition of Cr/Au (6/60 nm) in sequence as contact electrodes. All electrical characterizations are performed at room temperature in a vacuum chamber with pressure lower than 10$^{-5}$ Torr, and the electrical properties are measured using a Keithley 4200-SCS system. A representative optical photograph of a SnSe$_2$ FET is shown in Figure 2(a). To evaluate the contact resistance, both two- and four-probe measurements are performed. As shown in Figure 2(b), a good linear relationship between the current and bias voltage indicates a good Ohmic contact between Cr/Au electrodes and the interface of SnSe$_2$. Moreover, the coincidence between two- and four-probe measurements suggests a low contact resistance.

We can derive the threshold voltage $V_T$ by extrapolation of the linear part of the transfer curve according to the equation: $I_{SD} = (W/C_V SD/L) \times (V_G - V_T)$. The $V_T$ of the device on SiO$_2$ is about $-305$ V. We can calculate the area density of electrons in the SnSe$_2$ flake by $Q = C_{SiO_2} V_T / e$, about $2.2 \times 10^{13}$ cm$^{-2}$, where $C_{SiO_2} = 11.5$ nF cm$^{-2}$. It is too high to modulate with 300 nm SiO$_2$ as dielectric medium. To deplete the excess electrons in SnSe$_2$, we further adopt 70 nm HfO$_2$ as the back gate insulator. The HfO$_2$ is deposited onto p$^+$ Si substrate by atomic layer deposition (ALD). As shown in Figure 2(d), the current on/off ratio is just beyond 10$^4$, even though the dielectric constant of HfO$_2$ (25) is 5 times higher than that of SiO$_2$ (3.9). If we consider the SnSe$_2$ channel as 2D electron gas with area carrier density $2.2 \times 10^{13}$ cm$^{-2}$, the threshold voltage is determined as $-11.1$ V by $V_T = eQ / C_{HfO_2}eC_{HfO_2} = 316$ nF cm$^{-2}$. From the transfer curve in Figure 2(d), we can obtain the threshold voltage to be between $-12.5$ V and $-10.7$ V, which is consistent with the above assumption. However, when sweeping $V_G$ from $-16$ V to 10 V, unexpectedly, the device does not turn off at $-11$ V.

Therefore, it is unreasonable to simply consider the electron distribution in the SnSe$_2$ flake as 2D electron gas.
should be electrical potential difference along the vertical direction. According to semiconductor theory, if we want to deplete the excess electrons in the semiconductor, for the metal-insulator-semiconductor (MIS) structure, the thickness of the channel materials should be thinner than its maximum depletion width \( W_{\text{Dm}} \), which is determined as:\(^\text{18}\)

\[
W_{\text{Dm}} \approx \left( \frac{2e^{-k_0 \psi_{\text{inv}}}}{eN_D} \right)^{1/2},
\]

where \( \psi_{\text{inv}} \) is the surface potential when strong inversion occurs, \( N_D \) is the donor impurity concentration, \( e_0 \) and \( e_r \) represent vacuum and relative permittivity, respectively. For SnSe\(_2\), because of the shallow donor energy level, which is less than 25 meV below the conduction band,\(^\text{12,13}\) \( \psi_{\text{inv}} \) equals to the band gap (about 1 V) and \( N_D \) is equal to the electron density of SnSe\(_2\) at room temperature, about \( 2.2 \times 10^{19} \text{ cm}^{-3} \) (thickness \( \sim 10 \text{ nm} \)). The permittivity of SnSe\(_2\) along the c axis, \( \varepsilon_r \), is about 10.\(^\text{19}\) Therefore, \( W_{\text{Dm}} \) of SnSe\(_2\) is about 7 nm, which is smaller than the thickness of the flake. Naturally, there is no way to deplete the electrons only by the back gate modulation, regardless of how large the capacitance of the gate insulator is.

A natural way to modulate the transport of carriers in FETs is to apply a top gate using high-\( k \) dielectrics when the modulation of the back gate is not so effective. Therefore, we introduced a top gate to control the transporting electrons on the top surface of the SnSe\(_2\) device. A high-\( k \) top gate dielectric is fabricated by atomic layer deposition of HfO\(_2\). However, the SnSe\(_2\) cannot survive under the “harsh” deposition conditions. Even when we lower the deposition temperature to 150°C, the conductivity of the SnSe\(_2\) still increases at least two orders of magnitude after the deposition. Another widely used technique in tuning the transport of carriers in FETs is the use of an electrochemical gate (including ionic liquid and ion gel). It is much more effective than back gate (SiO\(_2\)) and polar-dielectric-based top gate (HfO\(_2\), Al\(_2\)O\(_3\), etc.), due to the formation of ultra-thin (\( \sim 1 \text{ nm} \)) double layer of ions, compared to that of back gate (\( \sim 300 \text{ nm} \)) and polar-dielectric-based top gate (\( > 5 \text{ nm} \)).\(^\text{20,21}\)

Here, we further adopt ionic polymer electrolyte as the top capping material in combination with 70 nm HfO\(_2\) on p\(^++\) Si substrate as back gate. The polymer electrolyte is applied by spin coating with filtered (pore size 500 nm) anhydrous methanol solution of polyethylene oxide (PEO) containing 20 wt. % LiClO\(_4\).\(^\text{22}\) Then, it is annealed at 100°C for half an hour in vacuum (50 Pa) to evaporate the solvents and solidify the electrolyte. A schematic diagram of such device is presented in Figure 3(a). Figure 3(c) gives the representative transfer curve of the SnSe\(_2\) FET under the modulation of ionic polymer electrolyte as top gate (iGate). Similar to the result of back gate in Figure 2(d), the current on/off ratio is about 1, and the device is not turned off completely by the iGate modulation, in spite of the high capacitance of the polymer electrolyte (above 1 \( \mu \text{F cm}^{-2} \)).\(^\text{23}\) However, with the covered polymer electrolyte, the current on/off ratio of a SnSe\(_2\) transistor increases from \( 10^4 \) to \( 10^8 \) using only back gate modulation, as shown in Figure 3(d).

The sweeping rate of the voltage is 10 mV/s. If we increase the sweeping rate to 100 mV/s, the high on/off ratio also disappears, indicating that there is ionic migration during the turn-off process.

Since there is only a back gate voltage bias applied during the measurement in Figure 3(d), what role of the covering polymer electrolyte plays in tuning the transport of carriers in SnSe\(_2\) FET remains a question. The leakage current between iGate and back gate is below \( 10^{-10} \text{ A} \), suggesting no short circuit occurs. A simple model considering the series capacitance of the HfO\(_2\) insulator and the polymer electrolyte is schematically shown in Figure 3(b). When the back gate is biased, an electrical double layer (EDL) is formed on the surface of HfO\(_2\) near the device, which actually functions same as the iGate and induces the formation of an EDL with opposite charged inner Helmholtz plane on the top surface of SnSe\(_2\) flakes. When the negative back gate voltage is applied, Li\(^+\) ions gather on the HfO\(_2\) surface near the flake and ClO\(_4^-\) assemblies on the top surface of SnSe\(_2\) flake, which deplete the electrons existing on the top surface of SnSe\(_2\) and the immobile ionized donors with positive charges are remained. With the help of the polymer electrolyte, the maximum thickness of SnSe\(_2\) flakes that can be modulated by the field-effect configuration increase from 7 nm to 14 nm, which covers the thickness scope of the flakes we used.

Additionally, when we increase the back gate voltage over 1 V, the current \( I_{\text{SD}} \) increases further and a turning point appears near 1.5 V, as shown in Figure 4(a). However, during the backward sweeping, \( I_{\text{SD}} \) does not decrease continuously but with steps. After the sweeping loop, the conductivity decreases three orders of magnitude. Repeating such a loop finally results in the death of the device. In Figure 4(b), Raman spectra are recorded both before and after the large positive gate bias. After the measurement, the peaks of vibration modes \( E_g \) and \( A_{1g} \) almost disappear, revealing an
irreversible structural transition has occurred in the SnSe2 flake. One possible origin of this transition is that Li+ ions intercalate into the interlayer of SnSe2 at large positive gate bias. To confirm this, we conducted the following control experiments. In Figure 4(c), the active area of the sample is covered by PMMA, with active area is covered by PMMA and a corner is exposed to polymer electrolyte, named sample A. (d) Transfer characteristic of device fully covered by PMMA, labeled as sample B.

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